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The analysis and modeling of fine pitch laminate interconnect in response to large energy fault transients

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The analysis and modeling of fine pitch laminate interconnect in response to large energy fault transients

by

Joel Arlen Jorgenson

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1998

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For the Graduate College

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ABSTRACT

In embedded applications, the miniaturization of circuitry and functionality provides many benefits to both the producer and consumer. However, the benefits gained from miniaturization is not without penalty, as the environmental influences may be great enough to introduce system failures in new or different modes and effects.

Of particular interest within this research is the effect of fault transients in reduced geometries of printed circuit card interconnect, commonly referred to as fine pitch laminate interconnect. Whereas larger geometries of conductor trace width and spacing may have been immune to circuit failure at a given fault input, the reduction of the trace geometry may introduce failures as the insulating effect of the dielectric is compromised to the point where arcing occurs.

To address this concern, a circuit card was designed with fine pitch laminate features in microstrip, embedded microstrip, and stripline constructions. Various trace widths and separations were tested for structural integrity (presence of arcing or fusing) at voltage extremes defined in avionics standard. The specific trace widths in the test were 4 mils, 6 mils, 8 mils, and 12 mils, with the trace separation in each case equal to the trace widths. The results of the tests and methods to artificially improve the integrity of the interconnect are documented, providing a clear region of reliable operation to the designers and the engineering community.

Finally, the construction of the interconnect and the results from the test were combined to create an empirical model for circuit analysis. Created for the Saber simulator, but readily adaptable to Spice, this model will describe high-speed operation of a propagating signal before breakdown, and uses data from the experiment to calculate threshold values for

the arcing breakdown. The values for the breakdown voltages are correlated to the experimental data using statistical methods of weighted linear regression and hypothesis testing.

1. STATEMENT OF THE PROBLEM

1.1. Introduction

As technology progresses in the electronics industry, a major emphasis towards miniaturization in hardware design is found at each discipline. From the component perspective, the solution has been large die designs with millions of transistors and waferscale integration. From the packaging perspective, integration of complex functions is accomplished with multichip module approaches, with either chips-first or chips-last designs. From the circuit board approach, functional density can increase greatly with minimal packaging approaches, such as direct chip attach (Figure 1.1), chip on board assembly (Figure 1.2), or ball grid arrays (Figure 1.3). Each of these solutions offers technical merit, as well as opportunities and challenges.

In all electronic equipments, advancements in processes and technologies allow the yields to improve and the capabilities to increase. However, the product environment remains unchanged, which may create difficult requirements for the design community to address. Whereas some mechanical influences decrease with the miniaturization of the product, the electrical and environmental conditions become more harsh and the product less tolerant. To ensure product quality, all requirements must be met without degradation.

Of particular interest within the electrical requirements is the ability for printed circuit card interconnect structures to perform without electrical or physical degradation in the presence of large voltage transients. In consumer electronics, these transients are power line fluctuations due to switching loads, surges from electric motors, or electric field coupling from external sources. In avionics, the primary concern is due to the coupling of large transients in the event of a lightning strike. In the latter case, the transient on the signal lines

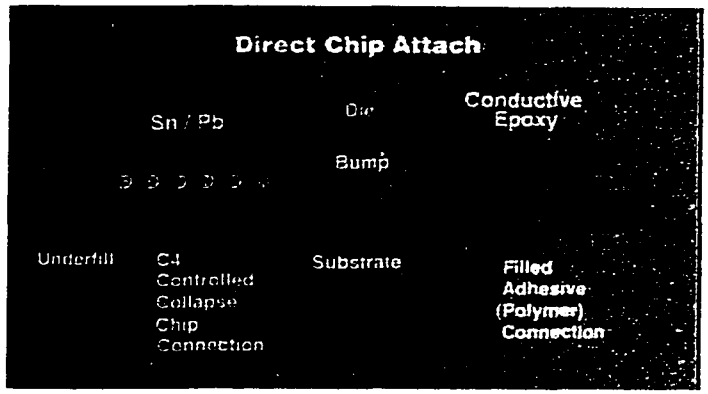

Figure 1.1. Direct chip attachment

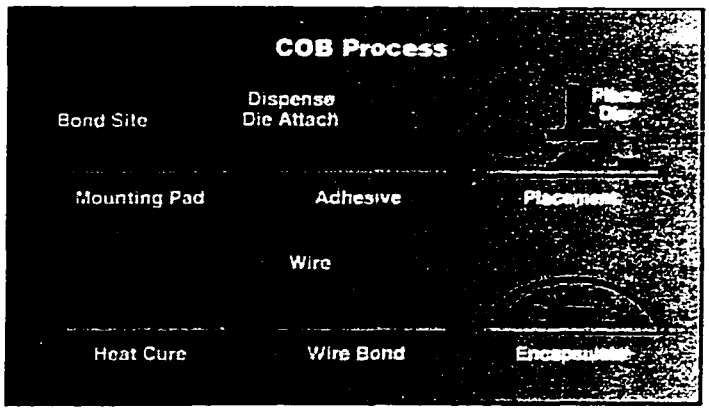

Figure 1.2. Chip on board (COB) attachment

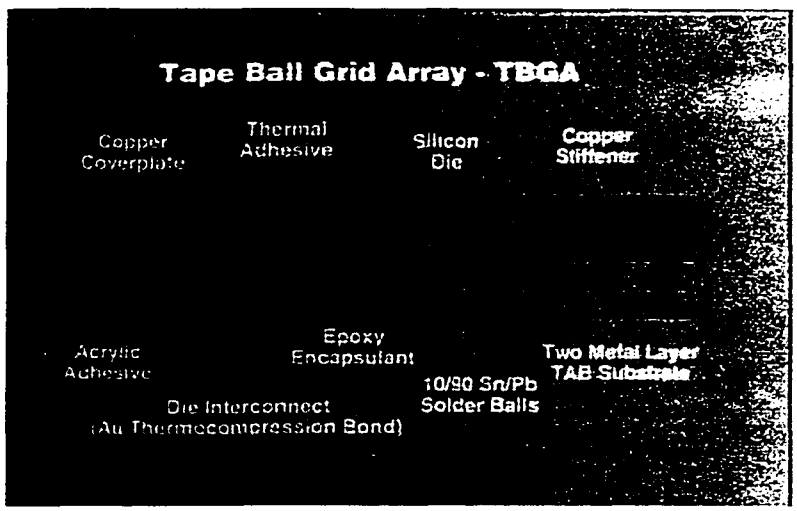

Figure 1.3. Ball grid array attachment

may rise to several hundred volts above nominal value, with current surges in excess of one hundred amperes.

Since the source of the transient is not directly connected to the circuits under consideration, the energy is transferred through the coupling of electric and magnetic fields by inductive and capacitive effects. To understand the mechanisms of energy transfer, an understanding of crosstalk must be attained, as well as an understanding of the sites of coupling (cable structures, adjacent traces, connector pins), and the mathematical relationship of the coupling at each site.

In traditional designs, the requirements for surviving such incidents have been satisfied by elaborate methods of shunting voltages and currents away from susceptible components, with verification testing performed to validate the design. In these instances, the interconnect is assumed to be reliable, modeled as an ideal structure with no resistive or reactive elements, and with infinite tolerance to such extremes. In the physical world, the assumption may not be accurate, and the survivability of such interconnect structures decreases with the shrinking of geometries, and changes with the structure of the interconnect design.

1.2. Research Objective

The proposed research is to characterize the response of interconnect structures using standard printed circuit card technologies and fine pitch geometries under high voltage transient conditions. The desired product of this research is: i) a defined limit for interconnect geometries in the presence of representative waveforms, ii) a methodology for ruggedizing the interconnect to such transients to improve survivability, and iii) the

development of an equivalent circuit model that will allow designers to simulate future circuits and designs.

A dedicated test structure has been designed and fabricated to analyze the response waveforms of high voltage stimuli decaying either exponentially or sinusoidally. The multilayer structure contains traces of different spacing, trace widths, and construction. In this context, the construction of the interconnect refers to the location of the return plane in reference to the signal. Stripline signals are located between reference planes; microstrip signals lie on the surface of the circuit card, with an air dielectric on one side, with the circuit laminate (and return plane) on the other; embedded microstrip is a microstrip signal that has some laminate dielectric between the signal and the surface. Figures 1.4 and 1.5 illustrate these constructions.

Because the fault mechanism(s) that induces the large voltage transients are external to the electronic system in which the printed circuit card reside, the nature and function of the electronic design have little to no effect on the magnitude of the transient input. Rather, the magnitude of the transient input is determined by the coupling of the fault and the cabling that connects the electronic system to external systems. In consumer products, the cabling may be household electrical lines, telephone lines, or television antennas. For avionics, the cabling is power distribution interconnect and system input/output wires.

Therefore, the tests defined for this research are not only applicable for the digital avionics systems developed for commercial and military aircraft, but also for commercial products with analog or digital components, such as televisions, video equipment, or computers. The waveforms from the avionics test procedure used in this research are representative of fault conditions found in consumer, industrial, or military applications.

For this research, first a review of the applicable research must be made, to determine the present understanding of the phenomena under consideration. The results of that effort are documented in Chapter 3. Next, the underlying principles of high-speed signal propagation must be described, in specific terms of crosstalk and transmission line behavior, discussed in Chapters 4 and 5. For the breakdown considerations, the ideas gathered in large structure designs for the breakdown of insulating materials is reported in Chapter 6. The experiment, results, and the construction of the model is the context of Chapter 7, followed by the stated contributions to the research community in Chapter 8. Finally, all materials and authors used as the foundations for this research are duly referenced in the bibliography.

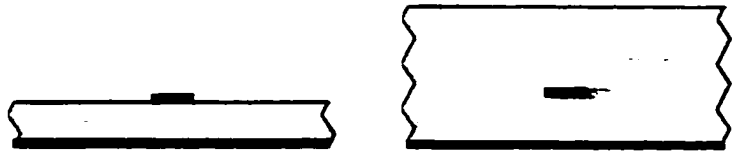

Figure 1.4. Microstrip and embedded microstrip transmission line

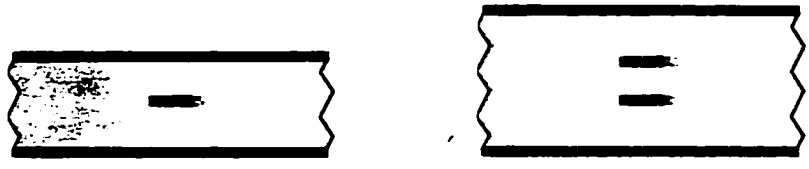

Figure 1.5. Centered stripline and dual offset stripline transmission line

2. GLOSSARY OF TERMS

2.1. Introduction

A glossary of terms follows. The descriptions are industry accepted standard definitions from signal integrity and advanced packaging.

2.2. Terms

Ball Grid Array: A packaging approach that places the interconnect of the package underneath the die in an array of surface mount solder bumps.

Capacitance matrix: A matrix containing the values for self and mutual capacitances for the signals in an interconnect structure.

Centered Stripline design: A stripline design that places the signal directly between the planes.

Characteristic impedance: The amount of current necessary to charge the capacitance between two points on a transmission line to a given voltage.

Chips-first: A multichip module approach that has the interconnect structure built upon the populated substrate.

Chips-last: A multichip module approach that places chips on a fabricated substrate.

Corona: The general class of luminous phenomena associated with the current jump to some microamperes at the highly stressed electrode proceeding the ultimate spark breakdown of the gap.

Crosstalk: The disturbance of a non-switching signal path by the switching of an adjacent signal path.

Dual Stripline design: A stripline design that places two signal layers between the planes.

Embedded microstrip: An interconnect design that places the signal trace embedded in the dielectric, with an embedded return path of much greater width either above or below.

Flip-chip: A packaging approach that places the pads on the bare die in contact with the package substrate, with the die substrate suspended in the air.

Inductance matrix: A matrix containing the values for self and mutual inductances for the signals in an interconnect structure.

Lossless structure: An interconnect structure that does not attenuate the signal.

Lossy structure: An interconnect structure that attenuates the signal.

Microstrip: An interconnect design that places the signal trace on the surface of the interconnect structure, with an embedded return path of much greater width than the signal path.

Minimal packaging: Packaging techniques that utilize minimal board space, such as flip chip or ball grid array technology.

Multichip module: A packaging technology that combines multiple bare dice on a substrate.

Product environment: The specified electrical, mechanical, and environmental requirements for a product.

Ruggedize: To increase the reliability of a product or a structure by reducing the susceptibility of failure due to environmental conditions. Normally associated with commercial off-the-shelf (COTS) products in industrial, military, or extended environments.

Stripline: An interconnect design that places the signal path between two return paths of much greater width than the signal path.

TEM (Transverse Electric/Magnetic): An approximation that states the generated electric and magnetic fields are only transverse to the signal path, and not longitudinal with the signal path.

Trace thickness: Height of the signal trace, usually measured in ounces of copper per square foot of circuit board. One ounce copper corresponds with a height of 1.4 mils.

Trace separation: Distance from edge of signal trace to the edge of nearest adjacent trace, usually measured in mils.

Trace width: Width of the signal trace, usually measured in mils.

3. LITERATURE REVIEW

3.1. Introduction

To date, the analysis and research of interconnect structures for single chip packaging, multichip module packaging, and printed circuit card laminates have restricted input voltages to operational conditions, and not overvoltage conditions. As such, the physical effects of extremely high currents (fusing of traces) and high voltages (arcing) have not been considered in present state of interconnect technology.

The research [3, 8-14, 17-18, 24] performed describing the transmission line behavior, inductive coupling, and magnetic coupling provide a solid basis to describe the interactions between conductive elements. Other work defining the progress made in simulation, modeling, and analysis [1-2, 5-7,15-16, 19-23] offer insight to multiple methods of describing the propagation of magnetic and electric fields through the interconnect medium. Additional research conducted in the distribution of high voltage power systems [29-36, 46, 48-55] offer necessary background in the corona and dielectric breakdown studies. The product of the research described in this document will further the knowledge of interconnect behavior and the ability to model the physical design.

3.2. Available Literature On Interconnect Theory

The study of interconnect for signal integrity and electromagnetic interference has received great attention in recent years. Researchers have made considerable progress in analyzing and modeling circuitry used in high speed design. As part of their efforts, the reflections of signals in transmission line structures are well predicted using quasi-TEM analysis, and can be accurately dampened using terminations calculated to match the characteristic impedances of the line and loading of the source and driver components.

For different configurations of interconnect design (microstrip, embedded microstrip, stripline), closed form solutions for characteristic impedance calculations have been derived. These calculations analyze cross-sectional areas of circuitry, using dielectric properties, trace thickness, trace width, trace separation, and vertical separation from return paths. In multi-layer printed circuit card design, the return paths are oftentimes ground and power planes, which are nearly indistinguishable from one another at high frequencies since the distributed capacitance between them results in a low impedance path between planes.

For the introduction of signals on non-switching lines located near active signal lines, the principles of crosstalk are examined in necessary detail in chapter 4. Theoretical responses as well as empirical results are discussed, with insight on crosstalk control methods that are part of the enhanced survivability techniques presented in this research.

Many of the principles that govern performance in high speed interconnect structures were developed nearly a hundred years ago when long distance electrical communication lines were established. The closed form definitions, known as the *Telegrapher's equations*, describe the voltage and current responses to a transmission line environment. These equations are discussed in necessary detail in chapter 5.

3.3. Available Literature On Interconnect Modeling

For accurate prediction of interconnect behavior in fine pitch multilayer printed circuit cards, computer simulation packages are employed. These packages are able to discretize the cross-section of the interconnect, describing the electrical properties of the physical structure in two-dimensional matrices (defined to be the *system matrices* of the interconnect) of capacitance and inductance. Because of the large number of elements found

in a cross section of a fine pitch multilayer printed circuit card, the size of the system matrices may be on the order of 10^5 by 10^5.

Where closed form solutions do not exist, multiple approximations methods are employed. Boundary element methods, finite element methods, and finite-difference time-domain methods are popular options to describe the complex geometries and fields of interconnect structures into mathematical equivalent definitions that can be characterized using Green's function, charge conservation, and other well established relationships.

3.3.1. Modeling Using BEM

Boundary element methods (BEM) have been widely applied to the calculation of electrostatic capacitance and inductance matrices for multiconductor transmission line systems. With BEM approaches, all conductor surfaces and dielectric interfaces are replaced by a charge distribution which exists in free space and produces a potential distribution equivalent to that of the original system. The principal advantages of BEM are its efficiency, simplicity of data preparation, and automatic handling of open regions. A major disadvantage of the BEM is the density of the system matrix, limiting the size of the design under consideration due to memory and processing constraints.

Greenfield is a commercially available package from Quantic Laboratories that performs interconnect modeling using BEM. Greenfield converts the total potential integral equations from the Green's function into a set of algebraic equations that can be solved using linear programming. The resulting matrix, generated using Galerkin's method [44,45], contains the node-point source distribution values and constraint conditions to maintain total system charge to zero. The field unknowns are located only upon conductors and dielectric surfaces in regions that are otherwise homogeneous. With this, elements need to be placed

on surfaces boundaries, and not throughout space (as in FEM). Discontinuities and irregular (non-linear) sections are discretized using second-degree, isoparametric, Lagrangian shape functions to express the total potential $\sigma(s)$ as a continuous function along all boundaries and interfaces. An example of BEM modeling with Greenfield is discussed as part of the transmission line modeling.

3.3.2. Modeling Using FEM

Finite element modeling (FEM) similarly discretizes the interconnect design into a mesh of homogenous elements. Arbitrary conductor configurations with curved geometries may be analyzed without difficulty and very large numbers of elements may be employed as the system matrix is sparse. However, mesh generation is more complex for FEM than for BEM, and for open-air problems it is necessary to truncate the mesh at a finite distance by introducing perfect electrical boundaries or perfect magnetic boundaries.

To analyze a design using FEM, the cross section must be "meshed" into homogenous elements. In two dimensional meshing, the discrete segments are often triangles, while three dimensional meshing usually yields tetrahedral elements. Each element is set to a singular value, and the system is analyzed through the integration of all elements. Figure 3.1 illustrates the meshing of a two conductor cross section using triangular elements. A commercially available software package utilizing FEM algorithms is Eminence from Ansoft.

3.3.3. Modeling Using FDTD

Finite-difference time-domain (FDTD) modeling uses the differential form of Maxwell's equations, discretizing the electromagnetic fields in both time and space. The differential form can be approximated using the center difference formulas. The electric and

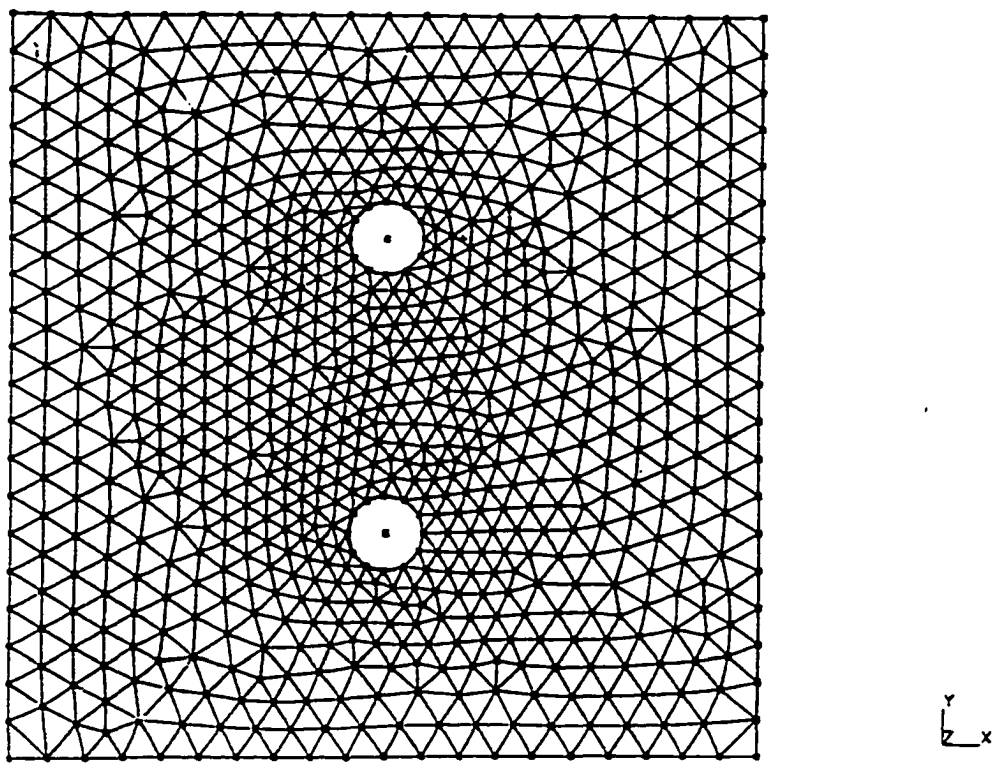

Figure 3.1. Meshing of a two conductor system using finite element modeling

magnetic fields (E and H) generated by the interconnect are discretized and relatively offset in both time and space. The future values of E and H are alternately updated every half of a time step. This method is known as Leap-Frog Time Integration. The spatial and temporal staggering of E and H are shown in Figure 3.2.

3.3.4. Commercial Modeling Packages

Implementations of the BEM, FEM, and FDTD methods are found in commercially available software packages from computer aided design developers, such as Quad Research's Quiet and Quantic Laboratories' Greenfield, or through consortiums, such as SRC's Aztec or TAP. Due to the complexity of implementing the functions described and

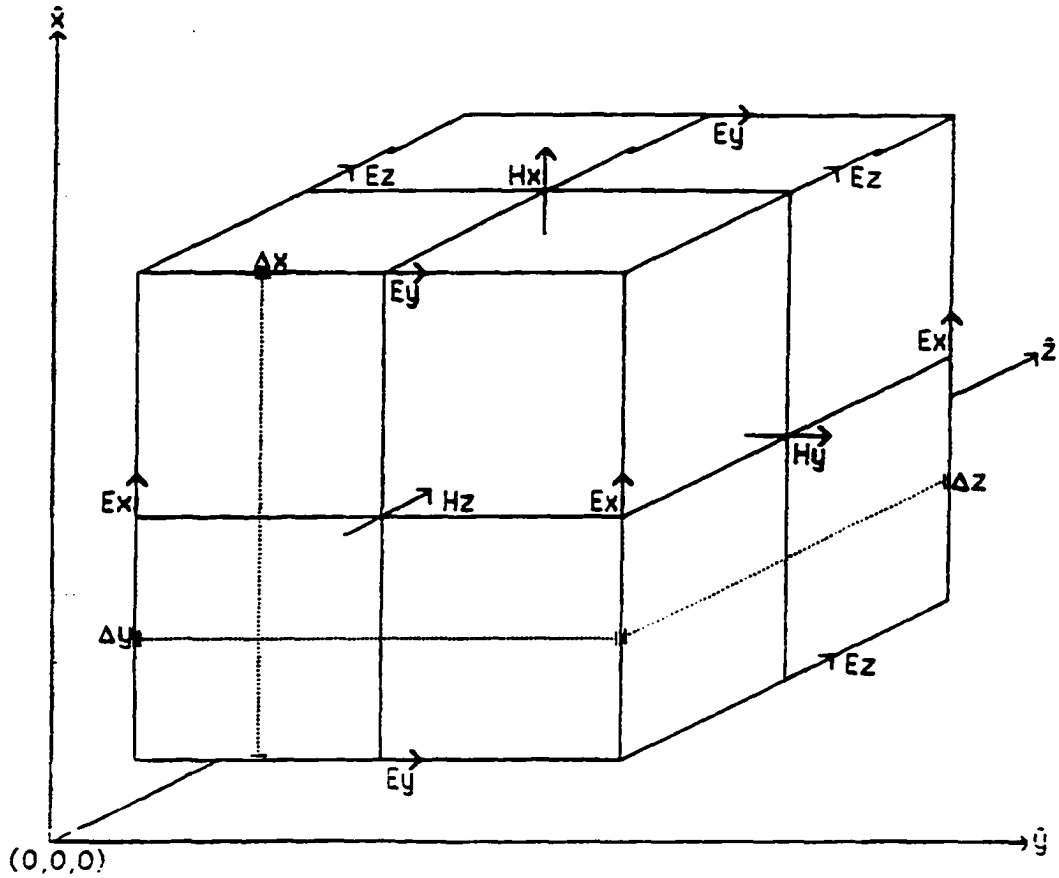

Figure 3.2. Discretization of a three dimensional system for FDTD

performing the necessary mathematics, the software packages are normally quite resource intensive and expensive. Lower cost solutions are available and are under development, but normally these attempts suffer in accuracy due to the assumptions made to simplify the computations.

3.4. Contribution of the Proposed Research

While all of the described techniques are appropriate for the analysis of a system within its defined operating limits, no models currently exist for the breakdown condition of interconnect in response to a large fault. In the proposed research, elements describing the

arc path may be added to the dielectric description, improving the model definition and allowing a single SPICE deck to describe the normal mode of operation as well as incorporating elements for a breakdown condition.

The capability to predict the transient behavior of the interconnect while large faults enter electronic systems is necessary to reduce time to market and development costs of advanced electronics. If accurate models are developed to analyze the S-parameters of the printed wiring structure, the potential to simulate improves the signal integrity, EMI, and TEMPEST margins.

The proposed research is directed to analyze the response of interconnect structures to large fault transients developed by internal sources, such as developed in-rush currents from systems starting or stopping, or from external sources, such as lighting strikes. The contribution of independent variables of the interconnect structure, such as trace widths, separations, and configurations (microstrip, embedded microstrip, and stripline), to the resilience of the fault will be mathematically defined. This derivation will be used to develop simulation models of the interconnect structure that will be used in Saber simulations that will predict circuit operation and correlate empirical results from laboratory experiments from test structures.

4. CROSSTALK

4.1. Applicability Of Crosstalk Theory

To explain the introduction of the transient fault to the interconnect of the electronic system, crosstalk theory is used to describe the coupling of voltages and currents due to electric and magnetic fields. The fields, caused by the external faults, intercept the cabling of the electronic system, and transient signals are injected.

If the suppression of transient spikes is treated as a crosstalk problem, the survivability can be enhanced by classic crosstalk control techniques. In this approach, the noise components are identified as source, victim, and coupling agent, with appropriate actions to reduce the source of the noise, eliminate the spurious coupling paths, and ruggedize the victim to increase immunity.

4.2. Introduction

The corruption of a signal by a neighboring switching signal, commonly referred to as *crosstalk*, may be a severe problem in circuit board design. If the victim of this disturbance is a signal particularly sensitive to noise, the reliability and the effectiveness of the design may be compromised due to problems associated with the layout. To address this problem, crosstalk and crosstalk control are discussed.

Crosstalk control techniques have been practiced in various degrees of success for quite some time. As with any control technique, the goal is to provide adequate assurances that the problem under consideration is addressed without significant overkill, measured in either component count, cost, or board area. The focus of this chapter is to provide background into the physics of the stated problem, discuss layouts susceptible to crosstalk,

and introduce techniques to resolve the problems. With the information presented, printed circuit cards can be designed immune to this problem.

4.3. Theoretical Background

High speed signals propagating through interconnect create electric and magnetic fields transverse to the direction of propagation, as shown in Figure 4.1. As these fields intersect other conductors, currents and voltages are introduced on the "quiet" or "passive" signals. The magnitude and pulse widths of the induced voltages and currents may be sufficient to cause false triggering in digital circuits, or introduce errors in analog circuits by varying the value of a voltage or current.

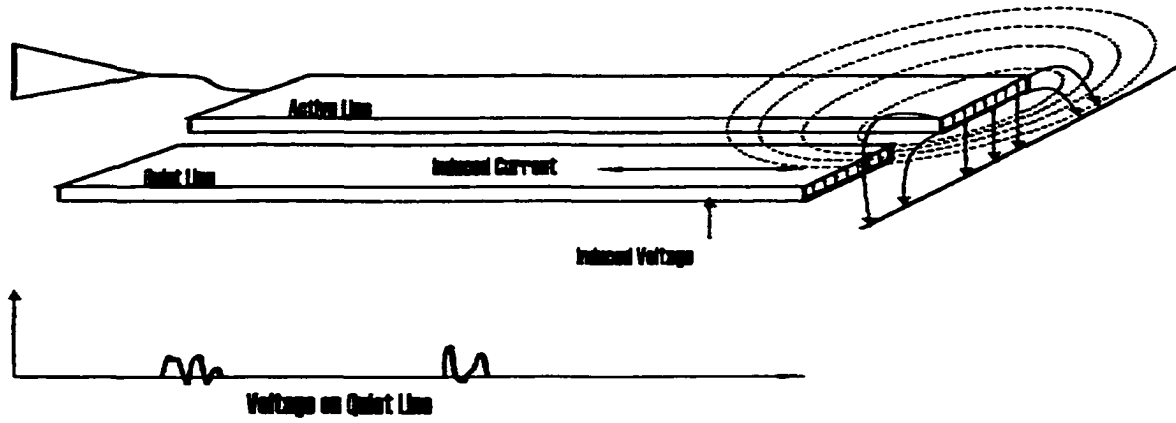

Figure 4.1. Introduction of crosstalk by induced fields

The induced current is created by a coupling of the magnetic field to the quiet line, and is directly proportional to the inductance of the interconnect; similarly, the induced voltage is created by the coupling of the electric field and is proportional to the capacitance. To determine the magnitude of the crosstalk, both inductive and capacitive coupling need to

be examined, and the concepts of near-end and far-end crosstalk are introduced. Figures 4.2 through 4.13 illustrate equipotential field lines in circuitry of different trace widths.

For reviewing the equipotential field plots, the lines surrounding the conductors illustrate the strength of the electric field from the active conductor. As the spacing between the field lines are increased, the strength of the electric field is decreased. As expected, the electric field strength is lessened (and subsequently, the spacing between the field lines is greater) at large distances from the conductor. For the quiet conductor (the conductor that is passive), the electric field strength is lessened with increased spacing, as expected from electromagnetic theory.

The effect of the dielectric is seen in the stripline and embedded microstrip constructions. The electric field strength at the passive conductor is lessened for these cases compared to the surface microstrip construction. This is due to the increased relative dielectric constant of the solid dielectric ($\varepsilon_r \cong 4.0$ for most materials) compared to $\varepsilon_r = 1$ for air.

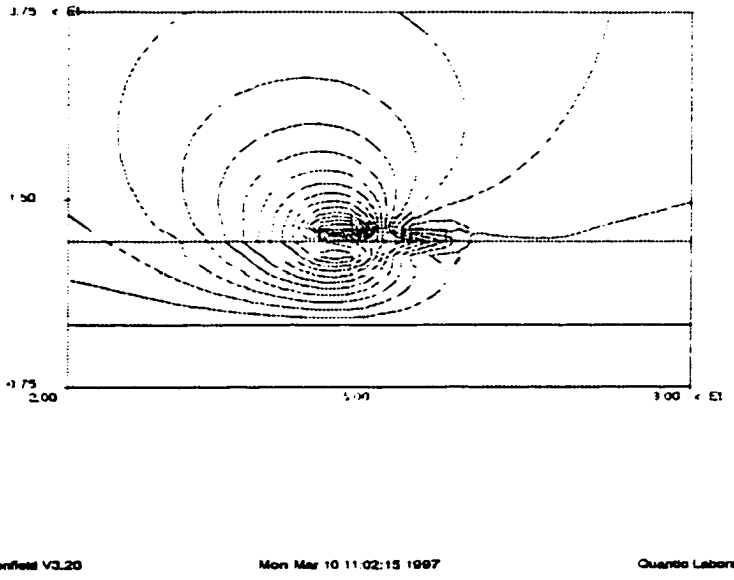

Figure 4.2. Field plot for 4 mil microstrip conductors with equal spacing

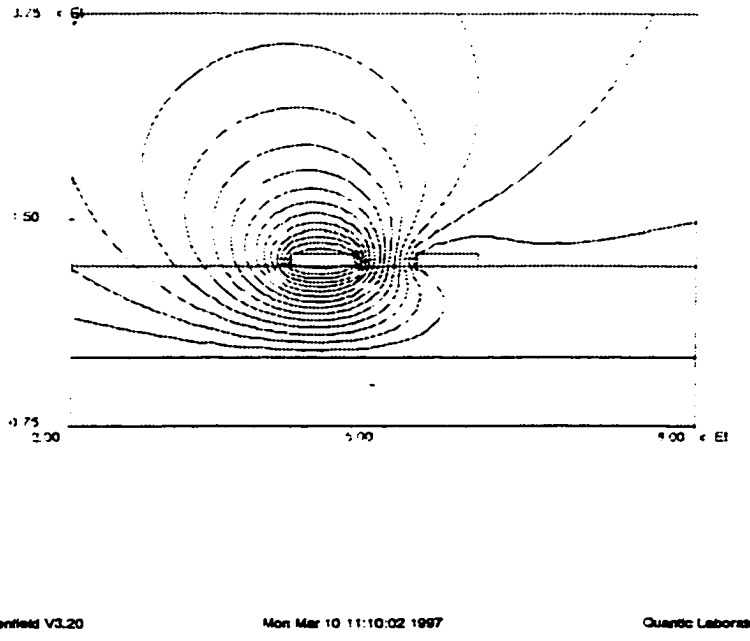

Figure 4.3. Field plot for 6 mil microstrip conductors with equal spacing

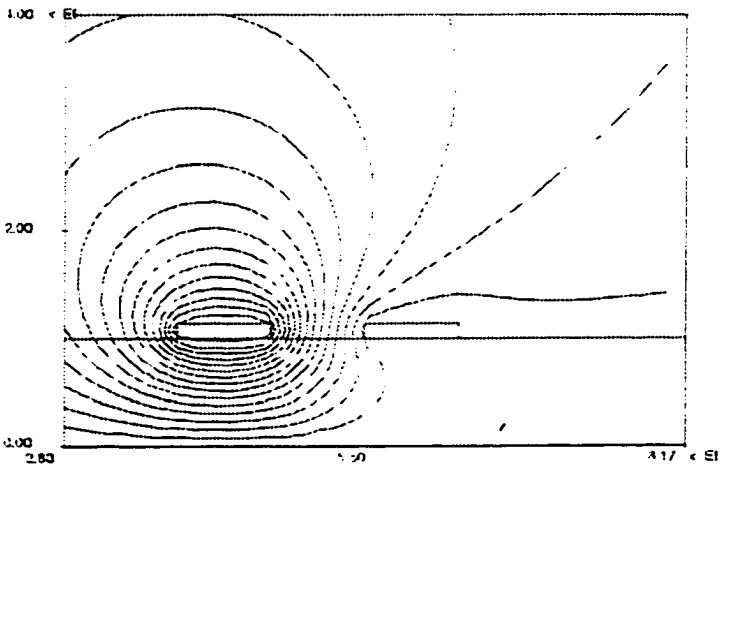

Figure 4.4. Field plot for 8 mil microstrip conductors with equal spacing

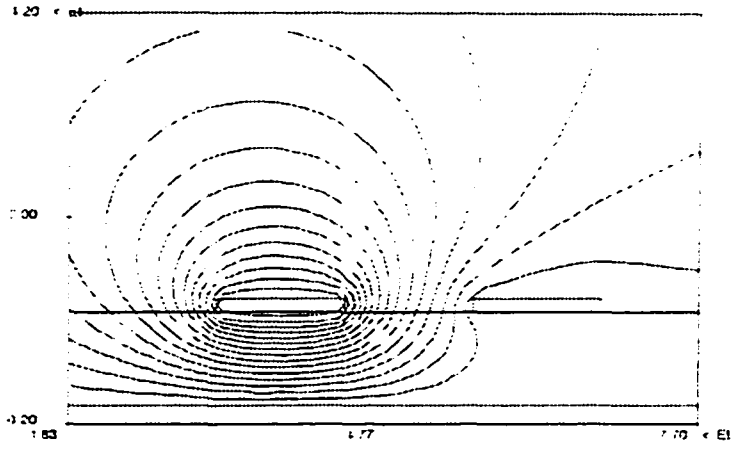

Figure 4.5. Field plot for 12 mil microstrip conductors with equal spacing

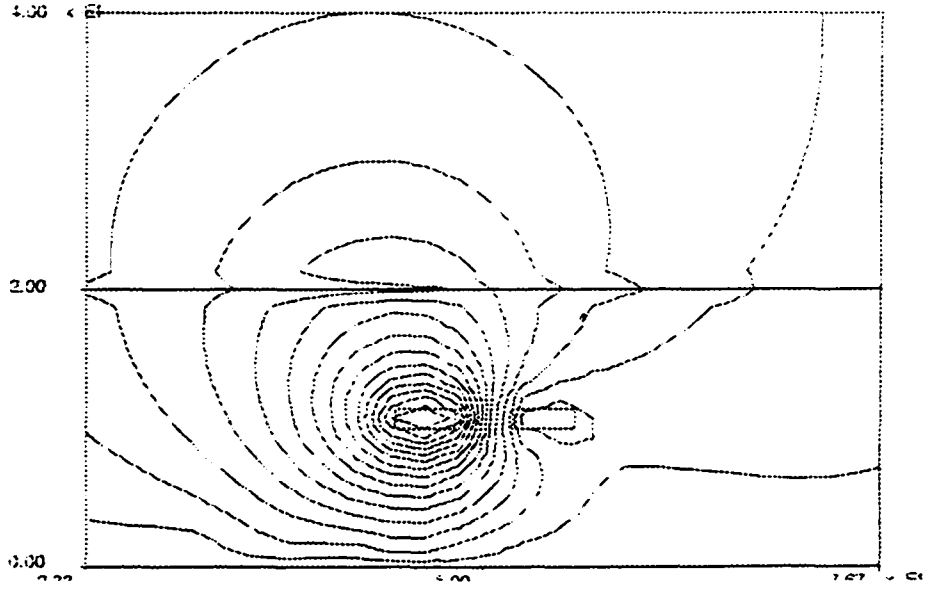

Figure 4.6. Field plot for 4 mil embedded conductors with equal spacing

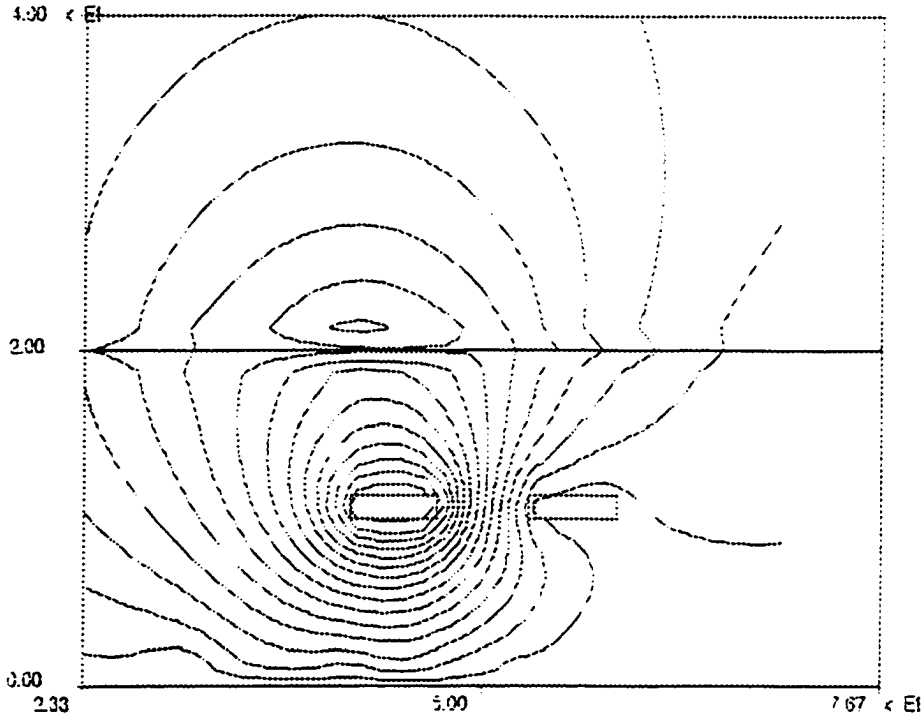

Figure 4.7. Field plot for 6 mil embedded conductors with equal spacing

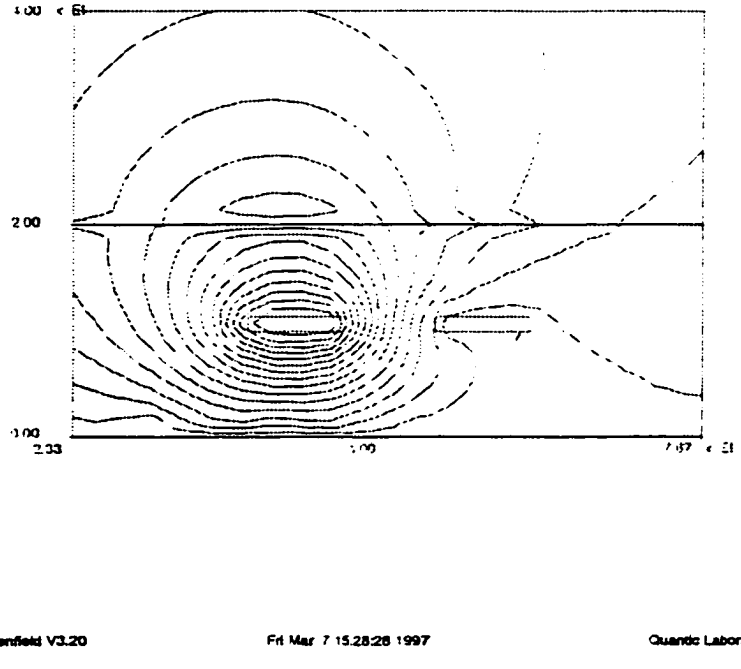

Figure 4.8. Field plot for 8 mil embedded conductors with equal spacing

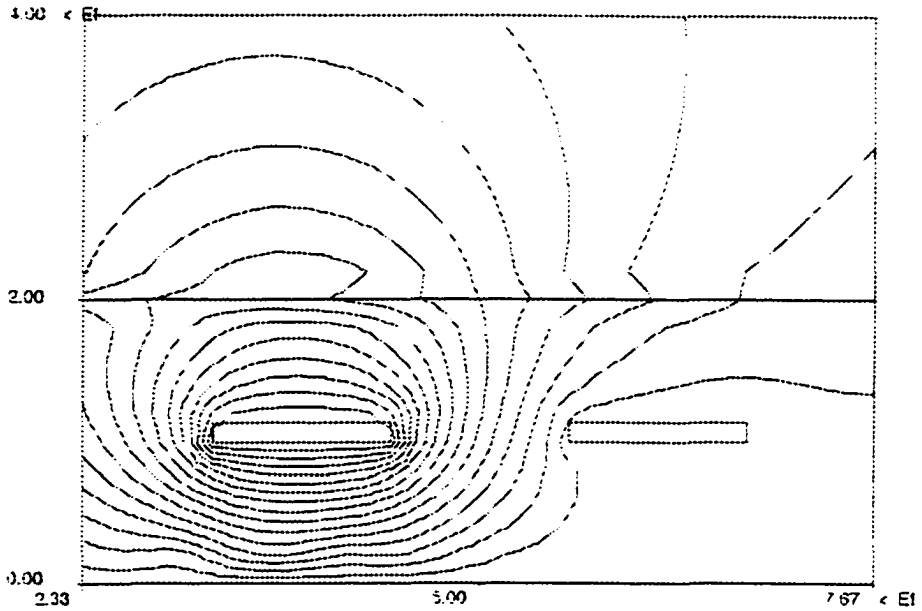

Figure 4.9. Field plot for 12 mil embedded conductors with equal spacing

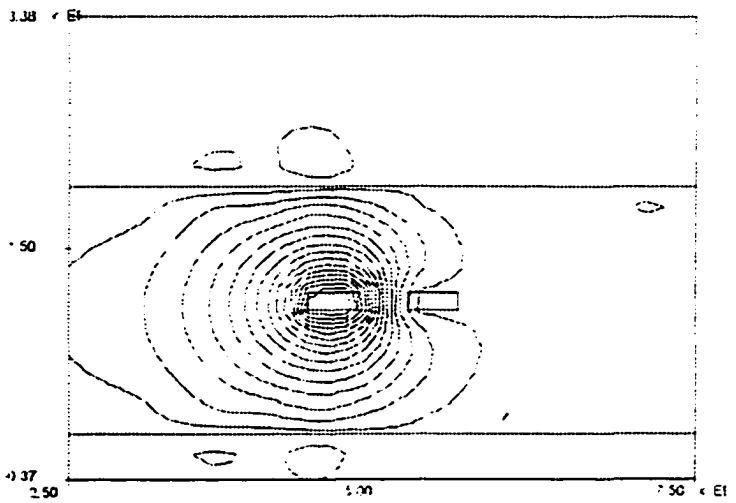

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Figure 4.10. Field plot for 4 mil stripline conductors with equal spacing

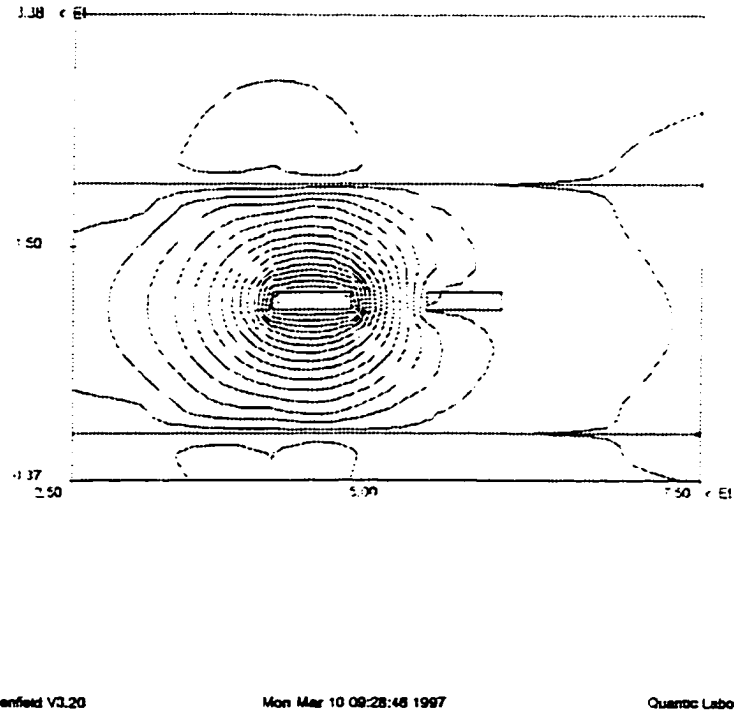

Figure 4.11. Field plot for 6 mil stripline conductors with equal spacing

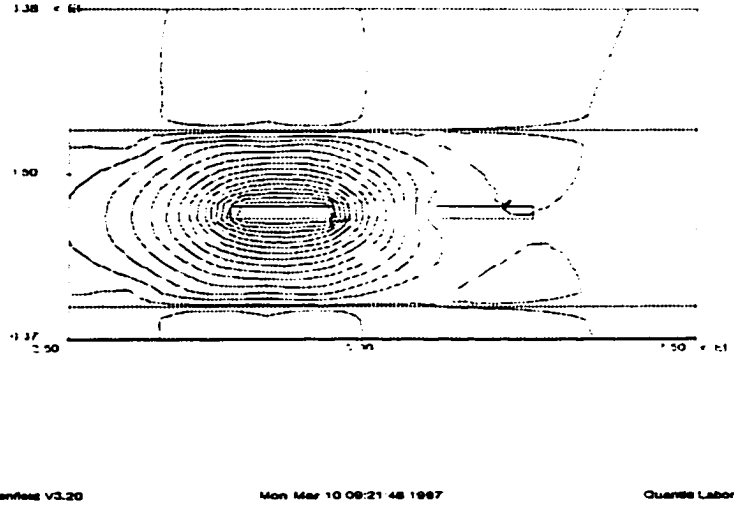

Figure 4.12. Field plot for 8 mil stripline conductors with equal spacing

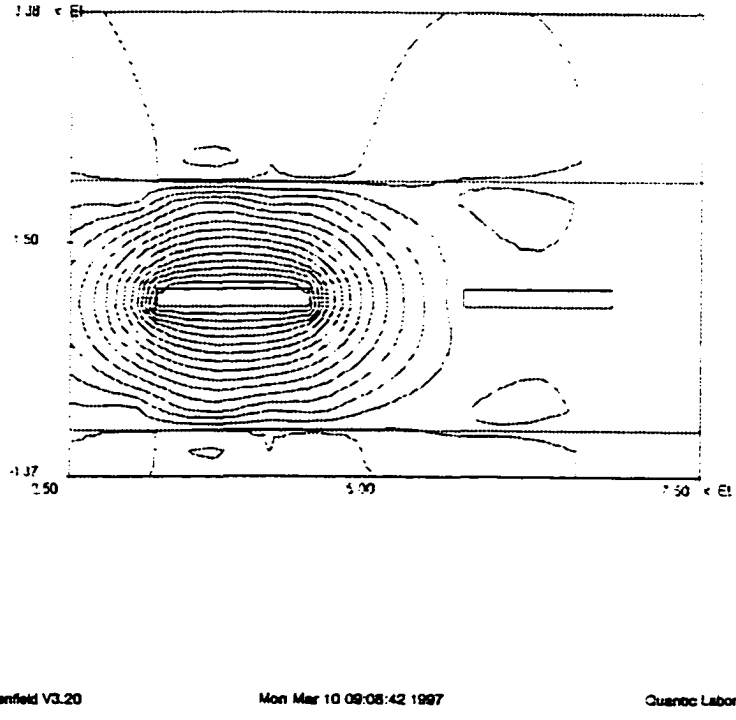

Figure 4.13. Field Plot for 12 mil stripline conductors with equal spacing

4.3.1. Forward and Backward Crosstalk Components

As stated in the introductory paragraphs, two signal traces in close proximity will have capacitive and inductive coupling. Each of these will be examined in following paragraphs, with individual contributions investigated. For the following discussion, consider the distributed transmission line illustrated in Figure 4.14.

Due to the mutual capacitive coupling, two equal and opposite currents, I_C, are induced on the quiet line by the transition of the active line. At the same time, an inductive current due to L_M is also induced but only in one direction. It travels in the opposite direction of the active line signal.

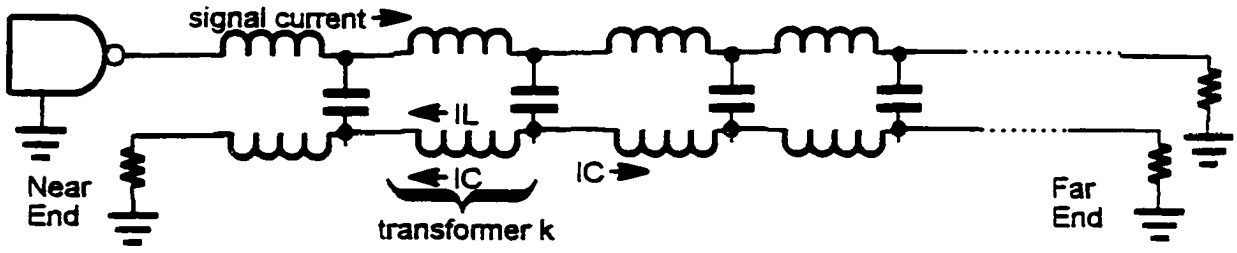

Figure 4.14. Mutual coupling between long transmission lines

At the source end of the passive line, I_C and I_L are additive. These summed currents produce a voltage drop in the same polarity as the source voltage. This voltage drop is termed "backward crosstalk" since it travels in the opposite direction of the source pulse.

At the far end of the passive line, I_C and I_L are of opposite polarity and thus subtractive. These subtractive currents produce a voltage drop termed "forward crosstalk" since it travels in the same direction as the source pulse.

Normally the forward crosstalk is opposite in polarity from the source voltage. This is the case in microstrip configurations whose field lines are in two different (non-homogeneous) dielectric materials, such as epoxy-glass and air. If both lines are completely surrounded by the same dielectric material (homogeneous), I_L and I_C have equal magnitudes and cancel at the far end [37]. This is why stripline configurations containing lines completely embedded in dielectric exhibit no forward crosstalk.

As the active pulse propagates down the active line, the forward pulse induced at a point propagates down the passive line, and is added to other induced forward pulses. These forward pulses continue to add directly on the passive line as the source wavefront travels down the active line. Therefore, when the end of the line is reached, the forward waveform

has an amplitude directly proportional to the length of the line and in opposite polarity to the signal voltage. Its pulse width is approximately equal to the source voltage risetime.

As the source voltage propagates down the active line, it also continues to induce backward crosstalk pulses. It generates the first one at the beginning of the line, and the last one at the end of the line. Thus, the string of backward pulses follow each other sequentially down the line towards the near-end where they add together. (The time required for the signal to propagate from the source to the load is defined to be the time delay of the signal.) The last backward pulse induced at the end of the line requires another time delay to travel to the beginning of the passive line. Therefore, the amplitude of the backward crosstalk component of electrically long lines is independent of the line length, and has a total width twice the total line delay.

4.3.1.1. Inductive Coupling Mechanism

Figure 4.14 represents a distributed lossless interconnection of active line with an adjacent static line. As the gate of the active line switches, the propagating magnetic fields induce voltages on the quiet line, as the distributed inductance acts as a succession of small transformers. As stated in the previous discussion, the induced voltage then propagates in backwards directions on the quiet line.

For the moment, consider only the segment defined by transformer *k*. When the voltage step on the active line arrives, the changing current induces a momentary voltage across transformer *k*. The voltage is the reaction of inductor *k* to a change in its current [27]:

$$V_M = L\frac{di}{dt} \qquad 4\text{-}1$$

The effect of the mutual inductive coupling acts only in the backward direction, as the total amount of coupling (total energy) spreads out over a period that is twice the path delay.

In practice, the reverse coupling smooth out into a rectangular function. If the lines were longer, the total mutual inductance would increase, and the reverse inductive coupling would increase in duration, but not magnitude.

4.3.1.2. Capacitive Coupling Mechanism

While the voltage induced in the magnetic fields propagates in only one direction, the electric field contributions propagate voltages in both the forward and backward direction. As the signal travels down the active line, the shunt capacitor between the active line and quiet line charges. Since the per-unit-length capacitance looking towards the source equals the per-unit-length capacitance looking towards the load, equal current flows in both directions.

For the moment, consider only the segment connected by capacitor *k*. The voltage potential difference between the quiet line and active line creates electronic charge to be stored momentarily in the capacitor [27].

$$Q = CV \qquad 4\text{-}2$$

From basic circuit theory, the charging or discharging of a capacitor will cause current to flow through the capacitor [27].

$$Ic = \frac{dQ}{dt} \qquad 4\text{-}3$$

In forward coupling, the mutual capacitance looks like the derivative of the input signal, and increases with increasing line length. In backwards coupling, the voltage will smooth to a rectangular function that saturates at a maximum value, but increases in pulse width with increasing line length.

4.3.1.3. Summation of Inductive and Capacitive Effects

As expected, the magnitude of the crosstalk is dependent on trace geometries, length of parallel signal paths, edge rate, dielectric properties, and voltage magnitude. The crosstalk also depends on the configuration of the interconnect structure: microstrip, embedded microstrip, or stripline. Formulas describing the backward and forward amplitudes are [41]:

For coupled line length < saturation length

$$V_F = K_F \frac{V * D}{A} \qquad 4\text{-}4$$

$$V_B = 2 * K_B \cdot \frac{V * D}{v_p * T_1}$$

For coupled line length ≥ saturation length

$$V_F = K_F \frac{V * D}{A} \qquad 4\text{-}5$$

$$V_B = 2 * K_B \cdot V$$

where V_F is the forward crosstalk voltage and V_B is the backward crosstalk voltage. The coefficients V, D, and A correspond with the transition on the active line, the length of coupled interconnect, and edge rate of the signal respectively. The K_B and K_F coefficients depend on the interconnect structure and are detailed in appropriate paragraphs.

The saturation length is a term to determine if the length is electrically "long". If the length of the coupled lines exceeds the saturation length, the magnitude of the backward crosstalk component reaches a maximum. The forward crosstalk component is directly proportional to the length of coupled lines, and does not have a defined maximum. Without matching terminations at each end of the passive lines, reflections will occur per the transmission line theory discussed in chapter 5. These subsequent reflections may be large enough to upset circuit operation, in addition to the original crosstalk waveform.

4.3.1.4. Microstrip Transmission Line

The first configuration under consideration is the microstrip, shown in Figure 4.15. The forward and backward crosstalk coefficients are related to the impedance of the signal lines and the mutual inductance and capacitance between them. Values for both can be derived from the following equations [41]:

$$K_B = C_o Z_o \frac{K_L + K_C}{4 * T_d} \qquad 4\text{-}6$$

$$K_F = -0.5 * C_o Z_o (K_L - K_C) \qquad 4\text{-}7$$

$$K_L = 0.55 e^{(-A_2 * B_2 * \frac{S}{H} \frac{W}{H})} \qquad 4\text{-}8$$

$$K_C = 0.55 e^{(-A_1 * B_1 * \frac{S}{H} \frac{W}{H})} \qquad 4\text{-}9$$

$$A_1 = 1 + 0.25 \ln \frac{(\varepsilon_r + 1)}{2} \qquad 4\text{-}10$$

$$A_2 = 1 + 0.25 \ln \frac{(u_r + 1)}{2} \qquad 4\text{-}11$$

$$B_1 = 0.1 \sqrt{(\varepsilon_r + 1)} \qquad 4\text{-}12$$

$$B_2 = 0.1 \sqrt{(u_r + 1)} \qquad 4\text{-}13$$

where S = trace spacing, H = distance from signal to plane, and W = trace width.

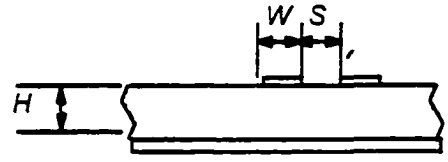

Figure 4.15. Microstrip profile

4.3.1.5. Embedded Microstrip Transmission Line

Next, following the presentation of the microstrip, the embedded stripline is discussed, as shown in Figure 4.16. The crosstalk equations for an embedded microstrip are similar to a microstrip line with the difference of a modified relative dielectric constant [41]:

$$K_B = C_o Z_o \frac{K_L + K_C}{4 * l_d} \qquad 4\text{-}14$$

$$K_F = -0.5 * C_o Z_o (K_L - K_C) \qquad 4\text{-}15$$

$$K_L = 0.55 e^{\left(-A_2 * B_2 * \frac{S}{H} \frac{W}{H}\right)} \qquad 4\text{-}16$$

$$K_C = 0.55 e^{\left(-A_1 * B_1 * \frac{S}{H} \frac{W}{H}\right)} \qquad 4\text{-}17$$

$$A_1 = 1 + 0.25 \ln \frac{(\varepsilon_r + 1)}{2} \qquad 4\text{-}18$$

$$A_2 = 1 + 0.25 \ln \frac{(u_r + 1)}{2} \qquad 4\text{-}19$$

$$B_1 = 0.1 \sqrt{(\varepsilon_r + 1)} \qquad 4\text{-}20$$

$$B_2 = 0.1 \sqrt{(u_r + 1)} \qquad 4\text{-}21$$

$$\varepsilon_{r'} = \varepsilon_r (1 - e^{-1.55 * \frac{H'}{H}}) \qquad 4\text{-}22$$

where S = trace spacing, H = distance from signal to plane, H' = distance from plane to top of dielectric, and W = trace width.

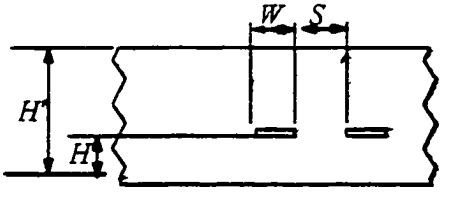

Figure 4.16. Embedded microstrip profile

4.3.1.6. Stripline Transmission Line

The last construction under consideration is the stripline design, illustrated in Figure 4.17. In the stripline design, the forward crosstalk element is equal to zero, since the $K_C = K_L$. The formula for the backward crosstalk component is similar to the microstrip, with a term included to account for the presence of an additional reference plane [41]:

$$K_B = \frac{2 * V_B}{V_i} \qquad 4\text{-}23$$

$$K_F = 0 \qquad 4\text{-}24$$

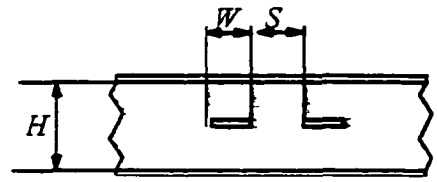

Figure 4.17. Stripline profile

4.3.1.7. Simulation of Crosstalk

For any active lines, there are multiple quiet lines that can be affected by the inductive and capacitive coupling effects. Similarly, for any susceptible line, there are multiple active lines that superimpose noise that may potentially destroy reliable operation. The above formulae discuss only the interactions of two lines, and extensions to the theory must be made to analyze networks of highly dense interconnect. As with transmission line analysis, crosstalk is a very complex mathematical problem that can only be adequately addressed by computer aided design software.

4.4. Crosstalk Susceptible Signals

Due to the nature of crosstalk, noise will be induced on traces adjacent to active, high-speed circuits. Accordingly, circuits that cannot tolerate the induced currents and voltages are most susceptible to crosstalk. Examples of circuits especially sensitive to the induced voltage levels include: analog-to-digital converter inputs, digital-to-analog outputs, and critical sense lines. Examples of signals especially sensitive to the edges introduced by the induced noise include: clocks, resets, and control signals (read enables, write enables, output enables). Figure 4.18 illustrates a signal with poor signal integrity, with noticeable overshoots, undershoots, and ringing.

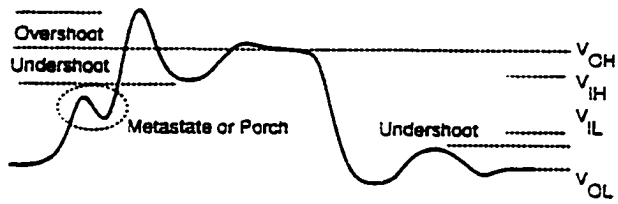

Figure 4.18. Overshoot and undershoot of a signal

4.5. Crosstalk Control Methods

When discussing the susceptibility of signals, the terms overshoot and undershoot are commonly used. Overshoot is the amount a signal passes it's DC target voltage. On a rising edge, overshoot is positive and on a falling edge, overshoot is negative. Undershoot is the amount of "ringback" after an overshoot (positive or negative). Overshoot can cause part damage or latch-up, while undershoot may cause double clocking or bad data setup.

Now that we have defined crosstalk, described the problems that crosstalk can introduce, and determined crosstalk magnitudes for forward and backward components, it is time to address minimization methods. Most of the methods used in crosstalk reduction are commonly used practices, and can virtually eliminate crosstalk problems when properly inserted.

Crosstalk, like EMI, is a problem when there exists a noise source (active line), transmission medium (induced magnetic and electric fields), and receiver or victim (passive lines intercepted by induced fields). Crosstalk can be controlled by removing any one of the three components. Although we cannot eliminate the noise source or victims, we can reduce the overshoots and undershoots of switching signals, which reduces excess energy normally seen as noise. Therefore, most crosstalk control techniques target a reduction or interruption of the coupling mechanisms.

4.5.1. Signal Separation

Figure 4.1 demonstrates the interception of passive signals by magnetic and electric fields of the active signal. As the distance from the active signals increases, the magnitudes of the fields decrease by the square of the distance. Thus, an obvious approach to reducing magnitudes of induced crosstalk is to increase signal separation. Figures 4.19, 4.20, and 4.21 [42] demonstrate the effectiveness the signal separation on crosstalk reduction for microstrip, dual stripline, and stripline configuration. Notice in the set of curves shown is the ratio of separation of lines to line width. In most designs, separation of three times the line width provides adequate protection to crosstalk.

A popular method for creating signal separation is to use guard strips, or ground strips, adjacent to critical signals. The effect of this technique is to shield the critical circuit

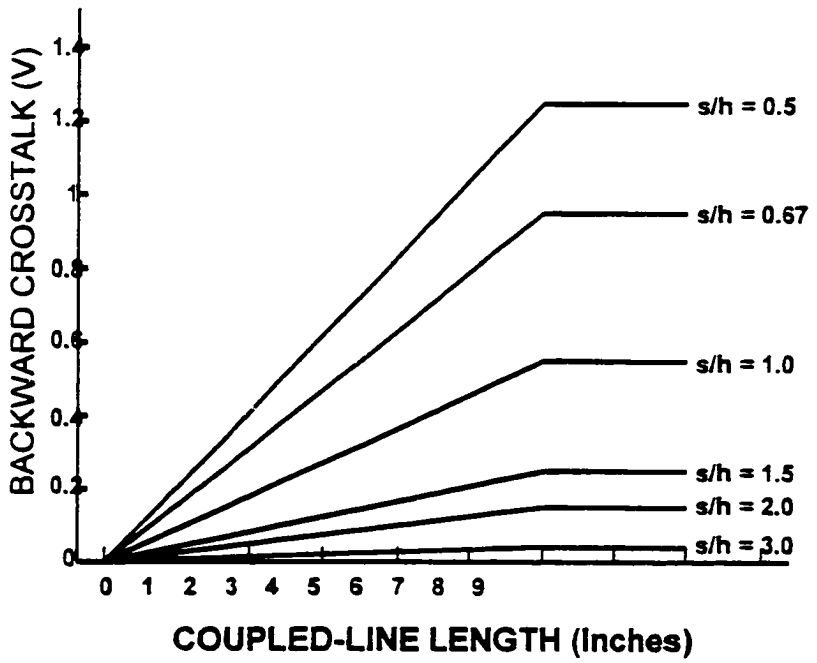

Figure 4.19. Backwards crosstalk in stripline circuitry

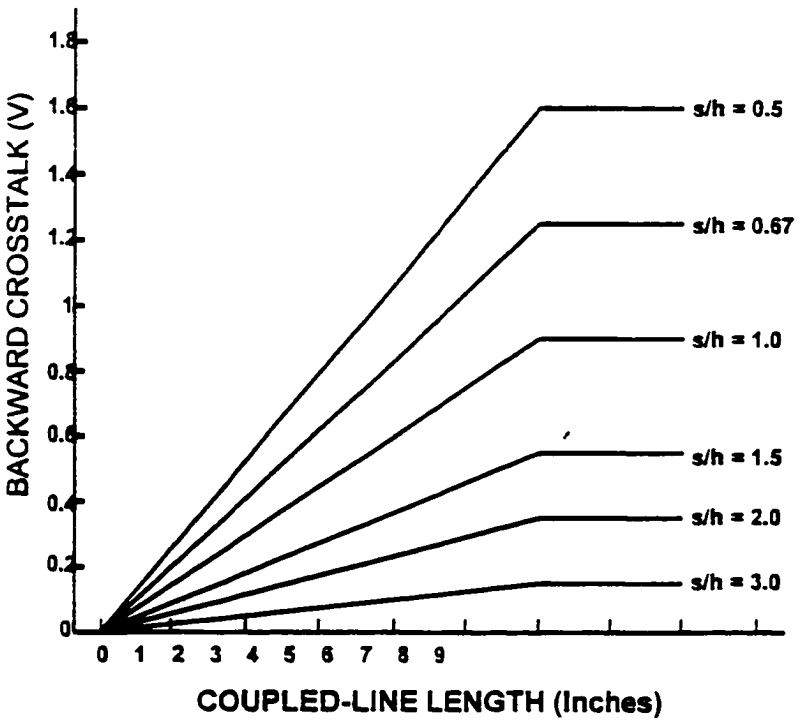

Figure 4.20. Backwards crosstalk in dual stripline

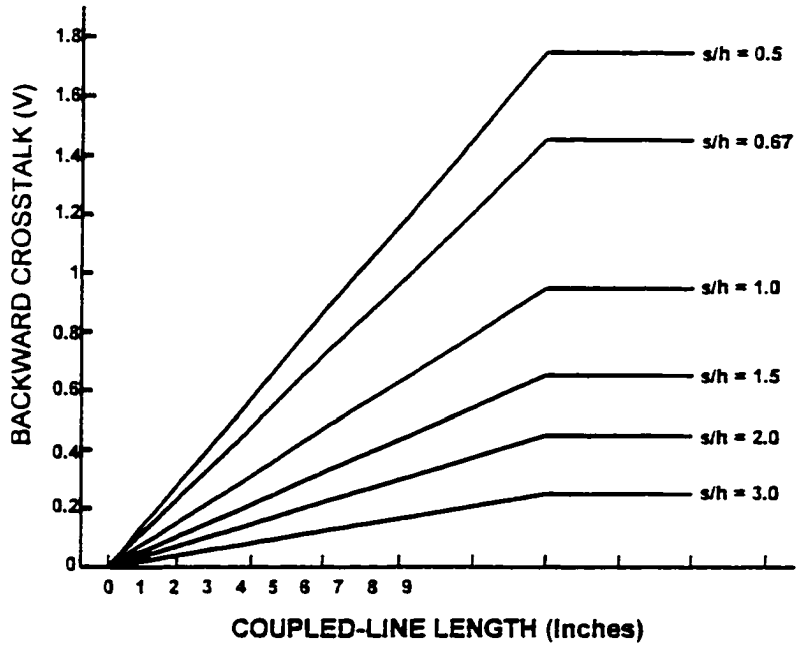

Figure 4.21. Backwards crosstalk in microstrip circuitry

from the interfering source. Essentially, any noise that may be created by the activity on the critical signal is coupled to a trace containing no receivers. The fields surrounding the guard circuitry trace (i.e., the fields created by the induced noise) are very weak, and little crosstalk is seen outside the guard trace. Hence, signals may be placed at minimum spacing next to the guard trace without concern over induced noise.

A few notes on guard strips. If the guard strip is connected to the reference plane in multiple places, a circuit path is created and current loops may exist. From a circuit analysis point of view, these loops are insignificant. The guard strips will have higher impedance than the ground plane, and will consequently have very little current flow. Therefore, guard strips do not need dedicated vias at regular intervals to reduce total inductance and limit current loop area.

The second effect is less obvious. By having a conductor at ground potential next to the critical signal, the characteristic impedance of the critical signal is lowered. In certain instances, this is unacceptable. Since the desired crosstalk control can obtained by increased spacing, one approach is to place a guard strip around the critical trace, complete the physical layout, and remove the guard strip before fabrication of the printed circuit card.

4.5.2. Coupled Length

As the equations in the earlier paragraphs indicate, a major contributor to the magnitude of crosstalk is the length of coupled lines. An obvious technique to control crosstalk magnitudes is to minimize the length that a susceptible signal parallels an active signal. This is necessary not only on the layer that the critical signal may occupy, but also layers above and below the critical signal not shielded by reference planes.

4.5.3. Layer Stacking

As mentioned in the previous paragraphs, crosstalk may occur from layer to layer, in addition to occurring within a single layer. It is not uncommon to have dielectric thickness thinner than or equal to minimum trace spacing. In this case, the signal will couple to signals on adjacent layers as well as signals on same layers. Figure 4.22 demonstrates such a layout. To address this, adjacent signal layers should contain perpendicular routes. Then, the coupled length of signals on adjacent layers will be the smaller of the two trace widths, which decreases the crosstalk to negligible amounts.

To eliminate layer-to-layer crosstalk for signals in the same direction, reference planes should be used as shields. The layout will have balanced (symmetric) construction, excellent impedance matching with the created stripline/microstrip configurations, and little to no crosstalk.

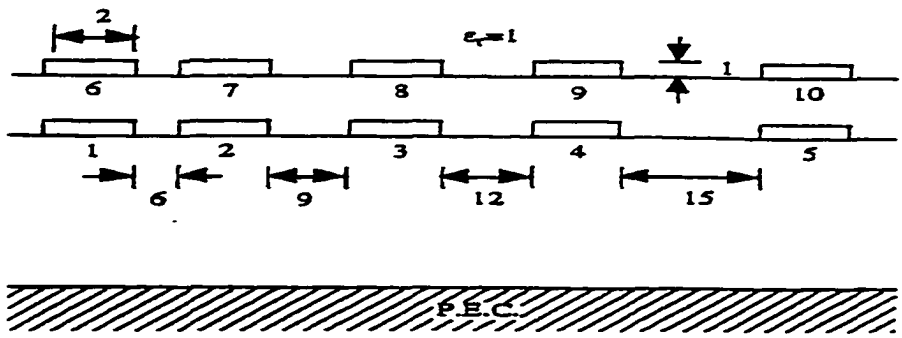

Figure 4.22. Interconnect structure with multiple signal layers

A common layer stack design is shown in Figure 4.23, with reference planes indicated by the solid lines. Shorter horizontal lines are routes of one direction (i.e., X direction), with the longer horizontal lines being the other (Y) direction. This orientation is effective in the reduction of crosstalk due to the elimination of parallelism of traces lying in opposite layers.

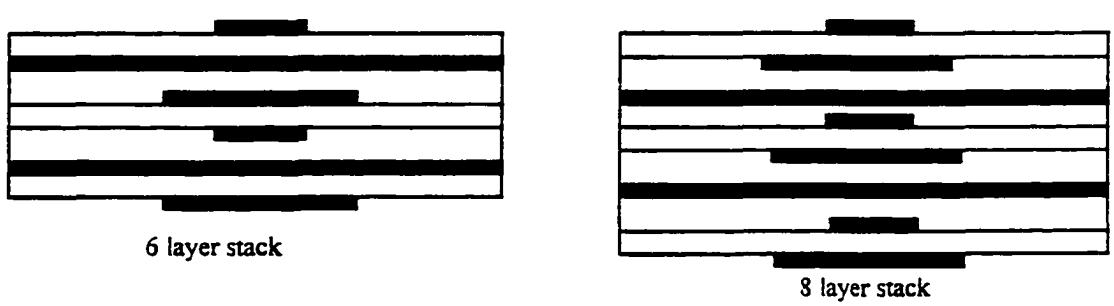

Figure 4.23. Layer stacking of 6 and 8 layer circuit cards

4.5.4. Connector Pin Assignments

Of course, high speed signals are not confined strictly to a single circuit card, and will often traverse through the system. Therefore, the issue of crosstalk in connectors must be addressed. As speeds increase, the selection of connector and interconnect becomes more

critical for performance, and requires careful attention from both the mechanical and electrical perspectives.

For simplicity, let's examine the four pin connector design shown in Figure 4.24. We will assign signals S1, S2, and S3 to pins 1, 2, and 4 respectively, and connect pin 3 to ground, which is the return path for each of the three signals. The loop (i.e., the path through the signal pin and returning through the ground pin) for signal S3 does not intersect the loops

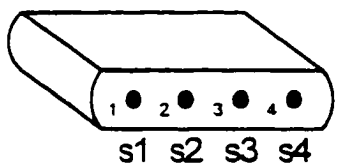

Figure 4.24. Four pin connector assignments

for signal S1 or S2. However, the loop for signal S1 completely encircles the loop for signal S2, and consequently the magnetic field created by signal S1 completely surrounds S2. The inductance created by this specific pin assignment is [37]:

$$Lx.r = 5.08H\ln\frac{c}{a} + 5.08H\ln\frac{b}{0.5D} \qquad 4\text{-}25$$

where a = distance from signal S1 to S2 (inches), b = distance from signal S2 to ground (inches), c = distance from signal S1 to ground (inches), H= pin length of connector (inches), and D = diameter of connector pin (inches.)

To reduce the crosstalk in the connector, the above formula gives guidance on several approaches. Separating the two signals will reduce the crosstalk, as will reducing the separation from signal to ground. An important conclusion from the second statement is that the poorest placement for ground pins within single row connectors is assignment to the

outermost pins. By placing multiple grounds at various locations within the connector, the effective distance from signal to ground is minimized. We have not discussed the other terms of the equation as the connector pin length and pin diameter are fixed parameters chosen in component selection.

While the above example demonstrates crosstalk in a single row connector, the same is true in multiple row connectors. Assigning ground pins in close proximity to signals is the best mechanism for reducing crosstalk on signals within the connector.

4.5.5. Split Plane/Partial Plane Design

Oftentimes, multiple power sources and return (ground) paths are required in a printed circuit card design. Analog and digital circuitry may be combined, ECL may be used with digital, or several different voltage levels may be needed. If the reference planes are split to accommodate the different supplies, crosstalk may be added in a subtle manner.

Recall that the return path will choose the route with least impedance, which translates to least inductance at high frequencies. In a current loop, the least total inductance is found to be the path with the highest mutual inductance to the signal path, since the total loop inductance is: [37]

$$L_{TOTAL} = L_1 + L_2 - L_M \qquad 4\text{-}26$$

where L_1 is the self inductance of the signal path, L_2 is the self inductance of the return path, L_M is the mutual inductance between the signal and the return.

To do this, the return path will attempt to "mirror" the signal path, and the return in the reference plane will lie primarily in the region of the signal path's projection. Normally this is not a problem, but may not be possible with split plane designs. In split planes, the deviation of the return current from the signal paths projection will cause the mutual

inductance to lower, which raises the total loop inductance. Since the inductive component of the crosstalk is directly related to the effective inductance, this deviation raises the value of the induced noise.

To combat this, the return path must be allowed to mirror the signal path, even if it means extending the signal path to follow the contours of the split plane design. While extending the signal path will increase the self inductance of that trace, the net effect is still reduced as the mutual inductance is still maximized.

4.6. Conclusion From Crosstalk Presentation

If the transient waveforms found on susceptible traces are caused internal to the electronic system due to large magnetic or electric fields, the survivability is greatly enhanced when crosstalk control mechanisms are implemented. In this manner, the transient value of current or voltage is restricted to the "active" signal only, and no victim signals are affected, or in severe circumstances, damaged.

By reviewing the principles of E and H fields propagating through free space, circuit board laminate, or other insulating materials, the interconnect structure may be designed to eliminate spurious coupling paths. The introduction of conducting shields, either additional or those necessary for proper circuit functionality, the orientation of signals normal to noisy traces, or proper spacing to reduce the magnitude of the intersecting fields are effective, efficient control methods.

5. TRANSMISSION LINES

5.1. Applicability Of Transmission Line Theory

To explain the magnitude of the incident waveform on the electronic system under consideration, transmission line theory principles are discussed. This provides theory on the waveform propagation, and the determination of the magnitude of the fault voltages and currents from the fault (lightning, etc.)

The waveforms that are caused by large energy faults have fundamental frequencies on the order of 10^7 Hz. While this is not necessarily fast in modern electronic systems, this frequency is reasonably fast when considering the external interconnect system the waveform propagates before encountering the electronics under consideration. Since the length from the fault source to the receiver is considered to be "electrically long", as given the formula [37]:

$$\lambda = \frac{f}{8} \qquad 5\text{-}1$$

where λ is the length of interconnect, and f is the frequency of the signal. With electrically long signals, transmission line principles simplify the circuit analysis, by considering the magnetic and electric field influences on voltage and current values.

5.2. Introduction

When analyzing circuitry for functionality, the interconnect is oftentimes regarded as a perfect electrical conductor (PEC) and a perfect magnetic conductor (PMC), with no loss and no associated fields. In physical designs, this is seldom the case, especially as frequencies increase, geometries decrease, and technologies advance. To properly analyze the system, the interconnect then must be viewed with its actual physical properties. To do this, the concepts of transmission line analysis are presented and discussed.

The principles of transmission lines govern the properties of the incoming voltages and currents from the external fault located at a distance electrically far from the electronic systems under consideration. To understand why the electronic system has little to no effect on the magnitude of the fault waveforms, the ideas behind the telegrapher's equations need introduction.

5.3. Definition

A *transmission line* is defined as any electrical transmission structure composed of at least two conductors. It may not seem obvious, but all printed circuit interconnect meets this definition. In fact, all but a very few specialized configurations, those consisting of a single conducting 'pipe' or *waveguide*, are transmission lines. Other very common examples include straight wire pairs, twisted wire pairs and coaxial cable. Thus the information presented in this chapter has utility in a wide variety of electrical engineering applications.

5.4. Configurations

Many practical transmission line configurations exist. Most, however, are variations of three generic types shown in Figure 5.1, wire over a plane, co-planar structures, or co-axial cables.

Two transmission line configurations are particularly useful in printed circuits: *microstrip* and *stripline*. Both are examples of a wire over a plane. Microstrip consists of a thin conductor separated from a single reference plane by a dielectric. Stripline consists of a thin conductor embedded in a dielectric separating two reference planes. Figure 5.2 and Figure 5.3 illustrate two slight variations of each.

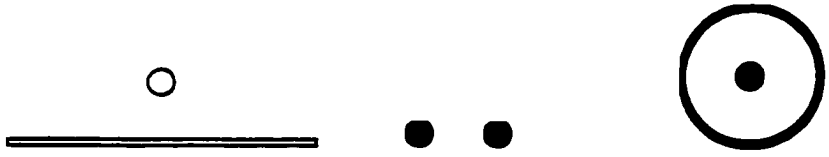

Figure 5.1. Common transmission line configurations

Figure 5.2. Microstrip and embedded microstrip transmission line

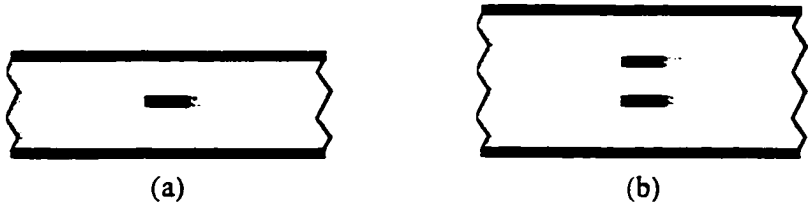

Figure 5.3. Stripline and dual offset stripline transmission line

The reference planes may be either power or ground planes - both types are effectively at ac ground, separated by a relatively low impedance path. This same general configuration also effectively models 'white wires,' jumper wires added externally to correct misconnections within the board.

5.5. Transmission Line Analysis

Fundamental to *transmission line theory* is the concept of wave propagation. The wave may describe the electric or magnetic field surrounding the transmission line, or it may describe the voltage or current on the line. In all cases, the wave propagates down the line at a *propagation velocity* equal to or less than the speed of light, *c*.[27, 28]:

$$v_p = \frac{c}{\sqrt{\varepsilon_r}} \qquad 5\text{-}2.$$

The denominator is the square root of the *relative permittivity* of the material surrounding the line. In the world of printed circuits, the term *dielectric constant* is used interchangeably. The reciprocal of the propagation velocity is the *propagation delay*, t_p,

$$t_p = \frac{1}{v_p} \qquad 5\text{-}3.$$

A wave in any length of transmission line experiences a *time delay* as a result of its finite speed of propagation. The value of the delay is proportional to the length of the line, l, and inversely proportional to the speed of the signal,

$$t_d = \frac{l}{v_p} \qquad 5\text{-}4.$$

This means that, at all frequencies except dc, the wave amplitude along the line is not constant but varies with position. Furthermore, waves do not propagate in just one direction, but may 'bounce' back and forth many times between the terminations before reaching steady state conditions.

At low frequencies these electrical effects are negligible; the variation in amplitude with position and the time required for the reflections to reach steady-state values are both insignificant. In circuit analysis, the transmission line is adequately modeled as a zero impedance path. At high frequencies, however, the electrical effects are significant. The line does not behave as a zero impedance path. Instead, it behaves as an element with characteristics that depend heavily on the geometry of the line. The most important consequence of this fact is that in the circuit board development process, the circuit design and layout steps are not independent.

A complete treatment of transmission line theory encompasses both electromagnetic field and circuit analysis. The former offers considerable insight into the phenomena of guided wave propagation, but it is rather complicated and inconvenient for practical analysis and design. The paragraphs that follow emphasize the latter, presenting several useful transmission line circuit equations.

5.5.1. Electromagnetic Analysis

The electromagnetic problem - the solution of Maxwell's equations - for almost all practical transmission line configurations is not trivial; conformal mapping techniques or sophisticated computational algorithms are often employed. The field distributions completely characterize the line, but such a description is inconvenient for practical CAD based analysis and design.

The ideal transmission line supports as its fundamental mode a *transverse electromagnetic*, or *TEM*, mode. This mode has no field components in the direction of propagation, thus its field distribution is completely specified by the transverse field distribution. Practical line configurations with homogeneous cross-sections behave ideally; both variations of stripline are good examples. Microstrip, on the other hand, does not have a homogeneous cross-section and cannot support a pure TEM mode. For all frequencies of interest in this document, however, a quasi-TEM approximation is valid. Thus, the circuit equations developed below, which assume a TEM propagating mode, may be applied to both configurations with little modification.

5.5.2. Equivalent Distributed Circuit

An *equivalent distributed circuit model* provides the link between the electromagnetic field analysis and conventional circuit theory. The model divides the transmission line into

many short sections, each of length Δz. Each section is modeled as a lumped-element circuit, shown in Figure 5.4, consisting of series and shunt impedance.

Circuit values are determined by four *line parameters: L, C, R, and G.* Each is defined in Table 5.1. These values are typically computed using discretization methods, such as those discussed in the literature review. For this research, boundary element modeling was used to compute the values, using Greenfield from Quantic Laboratories. Other packages and other computation approaches will yield similar results. For simulation purposes, the discretized structures are easily analyzed in Spice, Saber, or other simulators that will accept multiple cascaded identical objects.

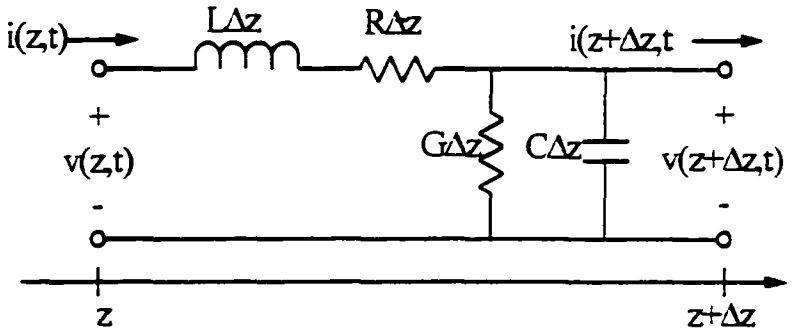

Figure 5.4. Equivalent distributed circuit model

Table 5.1. Line parameter definitions

Parameter	Definition	Units
L	series inductance per unit length	H/m
C	shunt capacitance per unit length	F/m
R	series resistance per unit length	Ω/m
G	shunt conductance per unit length	Ω^{-1}/m

The line parameters are related to the field distributions and in most cases are strong functions of frequency, the conductor and dielectric material properties, and the geometry of the configuration. The series inductance and shunt capacitance models energy storage in the magnetic and electric fields, respectively. The series resistance and shunt conductance represent loss mechanisms due to, among other things, a finite conductivity, the skin effect, and a nonzero loss tangent. These material properties also depend on several factors, including frequency and environmental conditions.

5.5.3. Circuit Analysis

This section summarizes the relevant transmission line circuit equations. The differential equations governing the electrical characteristics of an isolated line are derived and solved, then used to investigate the steady-state and transient behavior of a line arbitrarily terminated at both ends. In either case, the resulting equations describe the voltage and current on the line as functions of position and time. The analysis is strictly valid for *uniform* transmission lines operating in a TEM mode only: the cross-sectional geometry is of the line is homogenous and does not vary along the axis of propagation. This constraint should not limit the usefulness of the analysis since nonuniform structures, such as radial stubs and tapered lines, are not common in printed circuits, and all of the line configurations considered so far can support at least a quasi-TEM mode.

5.5.4. Voltage and Current Equations

An isolated transmission line of arbitrary length is shown schematically in Figure 5.5. The analysis starts by replacing the transmission line with the equivalent circuit of Figure 5.4. The goal is to develop expressions for two parameters, shown with the line, that will

completely specify the electrical characteristics of the line. Equations for the voltage and current on the line are expressed in terms of these parameters.

The application of Kirchoff's laws in the limit as $\Delta z \to 0$ to the equivalent circuit yields *telegrapher's equations* for the voltage and current:[27]

$$\frac{\delta v(z,t)}{\delta z} = -Ri(z,t) - L\frac{\delta i(z,t)}{\delta t} \qquad 5\text{-}5.$$

$$\frac{\delta i(z,t)}{\delta z} = -Gv(z,t) - C\frac{\delta v(z,t)}{\delta t} \qquad 5\text{-}6.$$

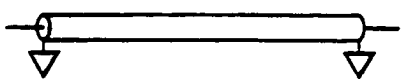

Figure 5.5. Isolated transmission line

These coupled partial differential equations are most often expressed in time-harmonic form: a time dependence of $e^{j\omega t}$ is assumed, the time derivative $\partial/\partial t$ is replaced with $j\omega$, and v and i become phasor quantities:

$$\frac{dv(z)}{dz} = -(R + j\omega L)i(z) \qquad 5\text{-}7,$$

$$\frac{di(z)}{dz} = -(G + j\omega C)v(z) \qquad 5\text{-}8.$$

The uncoupled versions are one-dimensional *wave equations* for the voltage and current on the line:

$$\frac{d^2v(z)}{dz} - \gamma^2 v(z) = 0 \qquad 5\text{-}9,$$

$$\frac{d^2i(z)}{dz} - \gamma^2 i(z) = 0 \qquad 5\text{-}10,$$

The parameter γ is the *propagation constant* of the transmission line. It is defined in terms of the line parameters:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}m^{-1} \qquad 5\text{-}11.$$

The real part of the propagation constant, α, is the *attenuation constant* of the line and is expressed in nepers per meter. A related quantity is the attenuation per unit length, given by:

$$e^{\alpha} = 20\log e^{\alpha} dB. \qquad 5\text{-}12.$$

The imaginary part of the propagation constant, β, is the *phase constant* of the line and is expressed in radians per meter. For a TEM mode, it is related to the wavelength by the relation.

$$\beta = \frac{2\pi}{\lambda} \qquad 5\text{-}13.$$

The general solution to each wave equation is a superposition of two traveling waves:

$$v(z) = V^{+}e^{-\gamma z} + V^{-}e^{\gamma z} \qquad 5\text{-}14.$$

$$i(z) = \frac{V^{+}}{Z_o}e^{-\gamma z} - \frac{V^{-}}{Z_o}e^{\gamma z} \qquad 5\text{-}15.$$

The term $e^{-\gamma z}$ represents the *forward wave*, a wave propagating in the positive z direction, while the term $e^{\gamma z}$ represents the *reverse wave*, a wave propagating in the negative z direction. The parameter Z_0 is the *characteristic impedance* of the transmission line and is also defined in terms of the line parameters:

$$Z_o = \sqrt{\frac{(R+j\omega L)}{(G+j\omega C)}}\Omega \qquad 5\text{-}16.$$

It equals the ratio of the forward voltage and current waves or the negative of the ratio of reverse waves. This definition is consistent with the concept of impedance in time-invariant signals and waveforms.

In the general case, the characteristic impedance and propagation constant are both complex numbers. Although the equations appear relatively simple, further analysis

necessitates the use of complex hyperbolic trigonometric functions. Furthermore, v and i above are phasor quantities. An explicit time dependence is regained only by multiplying each phasor by $e^{j\omega t}$ and taking the real part of the resulting expression. Fortunately, simplifying approximations exist that significantly reduce the computational effort.

5.5.5. Conventions

Several conventions dealing with the placement of the axis and the labeling of the terminations exist in transmission line analysis. They are presented here in an attempt to maintain compatibility with the texts available on this topic. The *load* is placed at the origin of the axis and the *source* on the negative axis l units from the origin. Figure 5.6 summarizes these details.

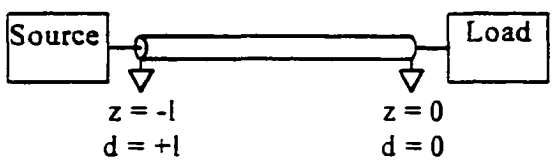

Figure 5.6. Labeling conventions

Most often a change of variables:

$$d = -z \qquad 5\text{-}17.$$

is performed to avoid the use of negative positions. The directions of the forward and reverse waves do not change - they are still defined with respect to the z axis, but the equations for v and i are slightly altered:

$$v(d) = V^{+}e^{-\gamma d} + V^{-}e^{\gamma d} \qquad 5\text{-}18.$$

$$i(d) = \frac{V^{+}}{Z_o}e^{-\gamma d} - \frac{V^{-}}{Z_o}e^{\gamma d} \qquad 5\text{-}19.$$

Unless otherwise specified, the analyses to follow assume these conventions.

5.5.6. Lossless Approximation

The transmission line is said to be *lossless* if it has no attenuation factors, either shunt or series. The line parameters R and G are both zero for an ideal lossless transmission line. In many cases this is a valid approximation to the real line, especially at frequencies where $\omega L >> R$ and $\omega C >> G$. The equivalent circuit consists only of series inductance and shunt capacitance. The propagation constant reduces to a purely imaginary number and the characteristic impedance reduces to a purely real number:

$$\gamma = j\beta = j\omega\sqrt{LC}m^{-1} \qquad 5\text{-}20,$$

$$Z_o = \sqrt{\frac{L}{C}}\Omega \qquad 5\text{-}21.$$

With the attenuation constant, α, equal to zero, the equations for v and i reduce to:

$$v(d) = V^+e^{-j\beta z} + V^-e^{j\beta z} \qquad 5\text{-}22,$$

$$i(d) = \frac{V^+}{Z_o}e^{-j\beta z} - \frac{V^-}{Z_o}e^{j\beta z} \qquad 5\text{-}23.$$

In the time domain these functions are simple sinusoids with arguments of the form $(\omega t \pm \beta z)$, with time and space variables.

5.5.7. Low Loss Approximation

The low loss approximation is valid when the line parameters R and G are both small. The term RG in the expansion of the propagation constant expression can therefore be neglected. Using a binomial expansion, γ is approximately:

$$\gamma = \alpha + j\beta \cong 0.5\sqrt{LC}\left(\frac{R}{L} + \frac{G}{C}\right) + j\omega\sqrt{LC}m^{-1} \qquad 5\text{-}24.$$

It is now complex, but the expression for β is identical to that of the lossless case. In addition, the determination of R and G may be avoided altogether for low loss lines by

computing α by mathematical techniques. This point is significant for computer aided analysis, since an accurate determination of these values from electromagnetic considerations is quite complex.

To determine the characteristic impedance, the lossless expression

$$Z_o = \sqrt{\frac{L}{C}}\Omega \qquad 5\text{-}25.$$

can still be used with high accuracy. Since the propagation constant is complex, the general expressions for the voltage and current do not simplify.

5.5.8. Steady State Solution

Expressions for the characteristic impedance and propagation constant have been expressed in terms of the line parameters, and equations describing the voltage and current in terms of these two parameters. What remains is the determination of the arbitrary constants V^+ and V^-. In mathematical terms, these are found by applying boundary conditions to the solutions of the differential equations. In this particular case, the boundary conditions are solved using Ohm's Law at the source and load.

The goal is to obtain two equations that uniquely determine the two constants. To do so, the source and load must be included in the analysis. Figure 5.7 shows the complete schematic. The quantities V_S and Z_S are the open-circuit voltage and output impedance, respectively, of the Thevenin source. The quantity Z_l is the input impedance of the load.

Two ratios are useful. The ratio of the forward voltage wave to the reverse voltage wave at any position, d, on the line is the *reflection coefficient*, Γ, at that position [27]:

$$\Gamma(d) = \frac{V^- e^{-\gamma d}}{V^+ e^{\gamma d}} = \Gamma(0) e^{-2\Gamma d} \qquad 5\text{-}26.$$

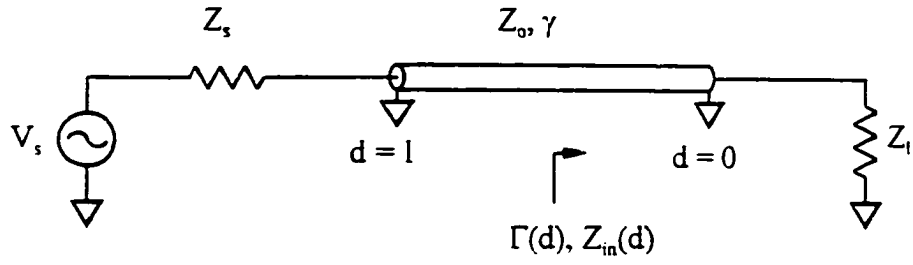

Figure 5.7. Transmission line with source and load terminations

The ratio of the voltage to current at any position, *d*, on the line is the *input impedance*, Z_{in}, of the line at that position [27]:

$$Z_{in}(d) = Z_o \frac{Z_l + Z_o \tanh \gamma d}{Z_o + Z_l \tanh \gamma d} \qquad 5\text{-}27.$$

The reflection coefficient and input impedance are not independent, but are related by

$$\Gamma(d) = \frac{Z_{in}(d) - Z_o}{Z_{in}(d) + Z_o} \qquad 5\text{-}28.$$

Note that both quantities are defined with respect to the load. That is, both 'look' toward the load. An arrow in Figure 5.7 shows this.

The two equations are found by simplifying the circuit at the source and load and applying basic circuit theory. Figure 5.8 shows the details.

Application of Ohm's Law to the circuit in Figure 5.8(b) yields the ratio of the coefficients in terms of the characteristic impedance of the line and the load impedance:

$$\frac{V^-}{V^+} = \frac{Z_l - Z_o}{Z_l + Z_o} \qquad 5\text{-}29.$$

This is nothing more than the reflection coefficient at the load, $\Gamma(0)$. A simple voltage division in the circuit of Figure 5.8(a) gives an expression for V^+ in terms of previous expressions [27]:

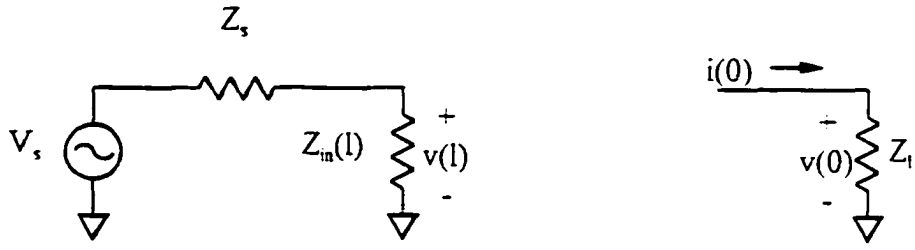

Figure 5.8. Circuit simplifications at the source and load

$$V^{+} = \frac{Z_{in}(l)V_s}{[Z_s + Z_{in}(l)][e^{\gamma l} + \Gamma(0)e^{-\gamma l}]} \qquad 5\text{-}30.$$

This completes the description of the steady state voltage and current on an arbitrarily terminated transmission line.

5.5.9. Transient Solution

While the steady state voltage and current are of some interest, the transient behavior of the voltage and current on transmission lines is much more important in digital circuit design. The transient response of a transmission line is primarily determined by its source and load termination impedances. Any *impedance mismatch* between a terminating impedance and the line's characteristic impedance causes a reflection from the termination. These reflections are the source of *reflection noise* - a significant problem in improperly designed digital interconnect.

An impedance mismatch may be characterized in terms of a *voltage reflection coefficient*, Γ, and a *voltage transmission coefficient*, T. The reflection coefficient is the ratio of the *reflected voltage wave* to the *incident voltage wave*. Note that this is just a generalization of the reflection coefficient defined above with the explicit orientation of the axis dropped. The transmission coefficient is the ratio of the *transmitted voltage wave* to the incident voltage wave. Both coefficients depend only on the line's characteristic impedance

and the terminating impedance [27]:

$$\Gamma = \frac{V_r}{V_i} = \frac{Z - Z_o}{Z + Z_o} \qquad 5\text{-}31,$$

$$T = \frac{V_t}{V_i} = \frac{2Z}{Z + Z_o} \qquad 5\text{-}32.$$

As expected, the two are not independent, but related through the equation

$$T = \Gamma + 1 \qquad 5\text{-}33.$$

Similar definitions exist for the current waves.

The initial voltage step is divided between the source impedance and the line's characteristic impedance,

$$V_o = \frac{V_i Z_o}{Z_s + Z_o} \qquad 5\text{-}34.$$

The voltage does not divide between the source impedance and the input impedance of line, as was the case in the steady-state, because no wave exists on the line and thus the source does not yet 'see' the effects of the load. The wave propagates to the load, where a reflected and a transmitted wave are created. The transmitted wave is dissipated or stored in the load. The reflected wave propagates back to the source, where another reflected and transmitted wave are created. The transmitted wave is dissipated or stored in the source. The reflected wave propagates to the load, repeating the cycle. These reflections are conveniently summarized in the *bounce diagram* of Figure 5.9. As the name indicates, the value of the voltage at any given time and at any given location is due to the summation of the incident voltage plus the "bounced" voltages due to reflections. This method of determining voltages at a given location is derived from the transmission line environments of long distance telegraphy.

The transient voltage response at the source and load are summations of the individual transmitted waves,

$$V(l,t) = \begin{cases} V_o, & 0 \le t \le \Delta t \\ V_o + V_o\Gamma_l T_l, & \Delta t \le t \le 2\Delta t \\ V_0 + V_o\Gamma_l T_l + V_o\Gamma_l^2\Gamma_s T_l, & 2\Delta t \le t \le 3\Delta t \\ \ldots. & \ldots. \end{cases} \qquad 5\text{-}35$$

and

$$V(0,t) = \begin{cases} 0_o, & 0 \le t \le \dfrac{\Delta t}{2} \\ V_o T_l, & \dfrac{\Delta t}{2} \le t \le \dfrac{3\Delta t}{2} \\ V_0 T_l + V_o\Gamma_l\Gamma_s T_s, & \dfrac{3\Delta t}{2} \le t \le \dfrac{5\Delta t}{2} \\ \ldots. & \ldots. \end{cases} \qquad 5\text{-}36$$

where the time interval is twice the time delay of the line,

$$\Delta t = \frac{2l}{v_p} \qquad 5\text{-}37.$$

Both of the series converge to the steady state values given previously.

The general transient response is a stair-step function much like Figure 5.10. Depending on the electrical characteristics of the line and the terminations, this function may exhibit several characteristics, each identified in Figure 5.10, that cause significant problems in digital circuitry. A *porch* may prohibit first incidence switching or cause double clocking. *Overshoot*, if severe enough, can cause latch up or damage to the part. *Undershoot* typically causes double clocking. Together, overshoot and undershoot are the cause of *ringing*.

As will be evident shortly, these characteristics are minimized or eliminated with properly designed interconnect. Alternately, poorly designed interconnect may be the cause of noise far in excess of the circuit's noise margins. These problems are difficult to diagnose

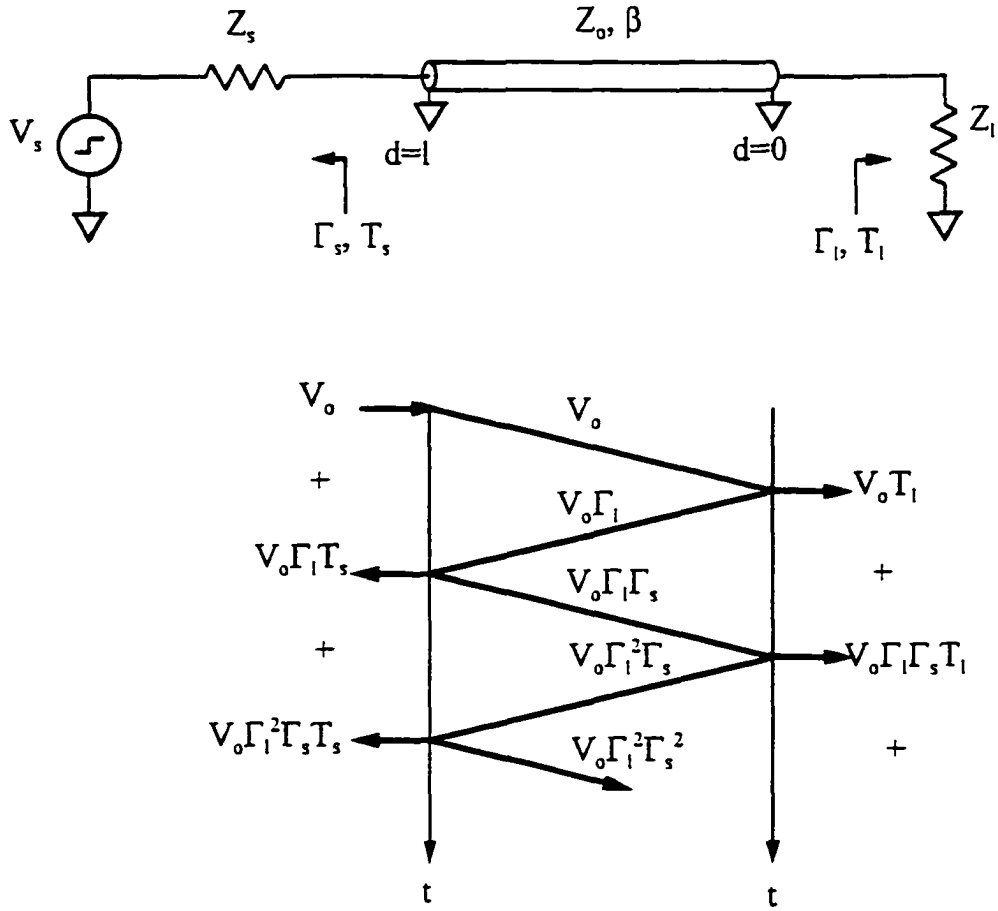

Figure 5.9. Bounce diagram

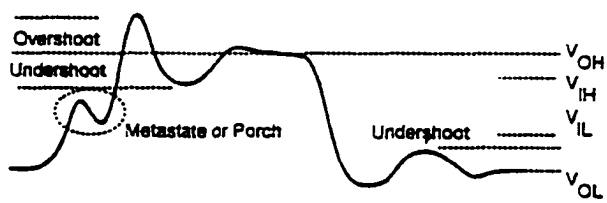

Figure 5.10. Typical transient response waveform

in embedded environments, and design improvements and enhancements are nearly impossible to implement once the board is designed.

The results of some Greenfield simulations should make this point clear. Each is a simulation of the schematic in Figure 5.11. The element 'TL' is a ten centimeter, fifty ohm, ideal transmission line model; it has a time delay of 0.7076 nanoseconds. The element 'VIN' is a five volt step with a one picosecond rise time. Table 5.2 lists the voltage input and the passive element values for each simulation.

Figure 5.12 is typical of circuits with a source impedance greater than the characteristic impedance, such as unbuffered CMOS outputs. The magnitude of the reflections are all positive. The waveform monotonically approaches the steady-state value of five volts, much like the response of an RC topology does. Depending on the values of the steps, a load may or may not switch at the incidence of the first wave.

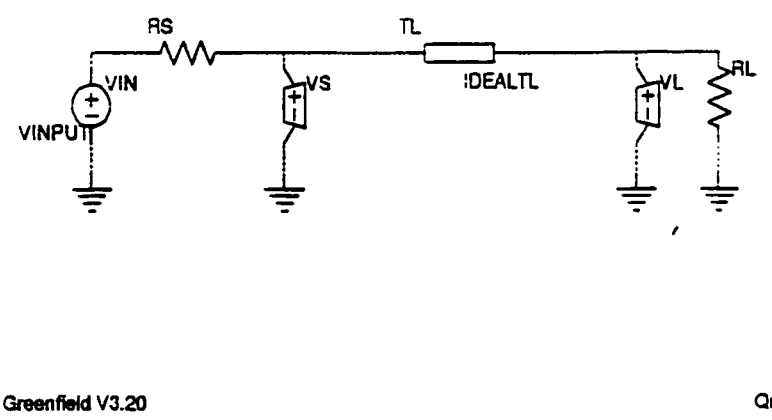

Figure 5.11. Greenfield schematic for transient response simulations

Table 5.2. Passive element values of Figure 5.11

Figure	V_S	R_S	Z_O	R_l
Figure 5.12	5 V step	150 Ω	50 Ω	infinity
Figure 5.13	5 V step	16.67 Ω	50 Ω	infinity
Figure 5.14	5 V step	50 Ω	50 Ω	infinity
Figure 5.15	5 V step	50 Ω	50 Ω	50 Ω

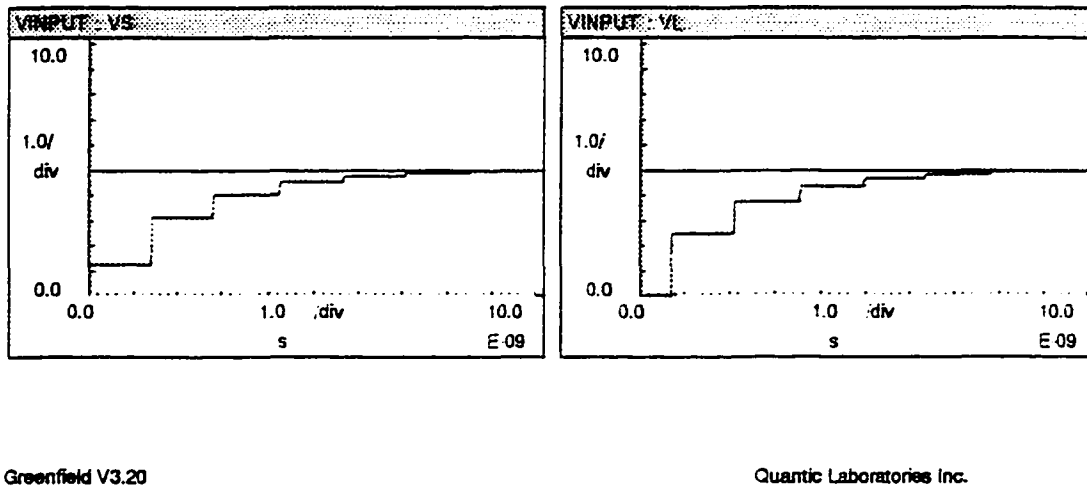

Figure 5.12. Transient voltage response of a line with high source impedance

Figure 5.13 is typical of circuits with a low source impedance, such as the ECL family and large TTL drivers. The magnitudes of the reflections alternate signs: the waveform rings before settling at five volts. Note that the magnitude of the overshoot and undershoot can be a significant fraction of the input step. In this case, the output may be stressed to conditions over rated specifications, and the interconnect mismatches may become a reliability concern.

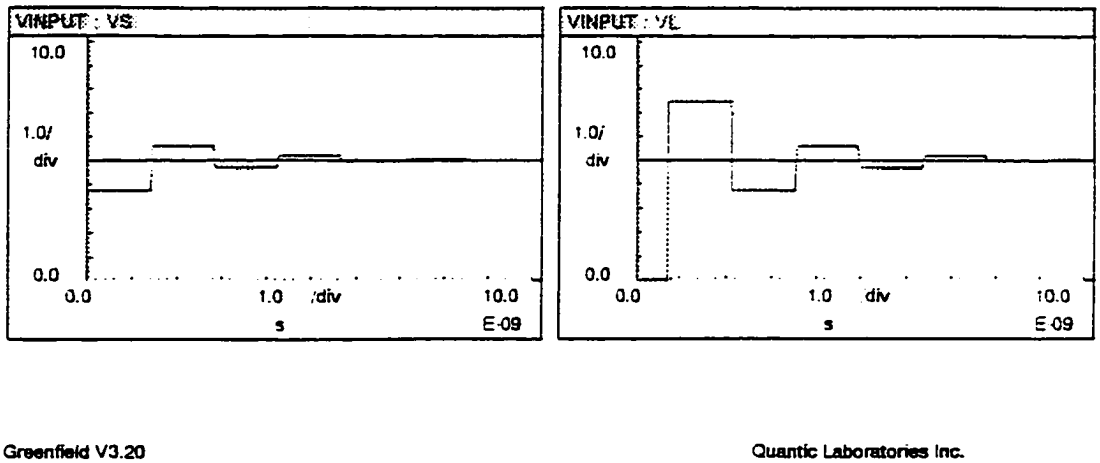

Figure 5.13. Transient voltage response of a line with low source impedance

Figure 5.14 shows the result of a matched source - the source impedance is equal to the characteristic impedance of the line. This configuration has desirable properties. The source waveform still has a porch, but the load waveform is simply a delayed version of the input. The source does not add reflection noise, since the reflection coefficient is zero from such a termination.

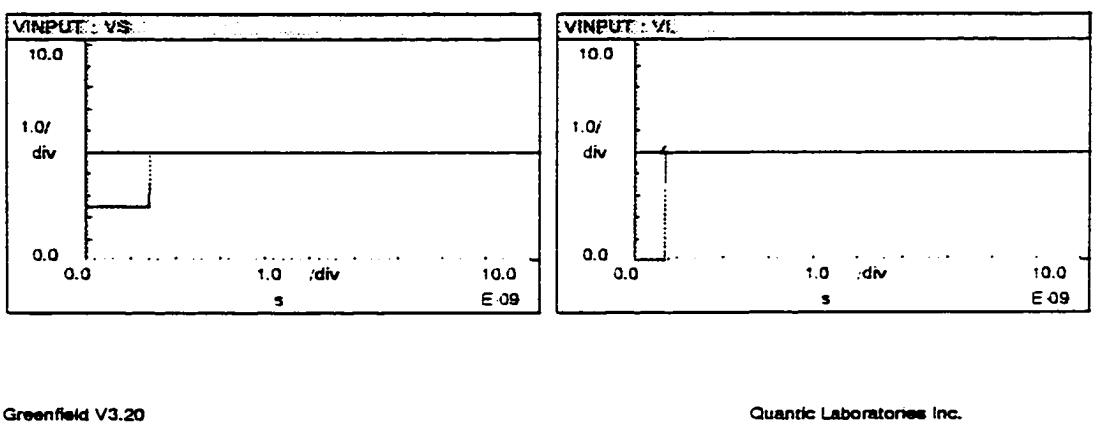

Figure 5.14. Transient voltage response of a line with a matched source

Finally, Figure 5.15 shows the result of a matched source and load - both terminations are equal to the characteristic impedance of the line. This configuration also has desirable properties. The transmission line 'looks' infinitely long, and the load waveform is a delayed and scaled version of the input. If the scaled value is greater than the high input threshold, the load switches at the incidence of the first wave.

The actual source and load impedances of digital circuits differ from family to family and are highly nonlinear, unlike these simple examples. Even though they do not exhibit the characteristics of any specific digital implementation, they do effectively illustrate several trends commonly seen in digital circuits. These illustrations are useful to designers trying to match estimated performance to representative source impedances and characteristic impedances of the printed circuit card network. As such, it may provide an initial baseline for predicted operation and insight on the need of terminations.

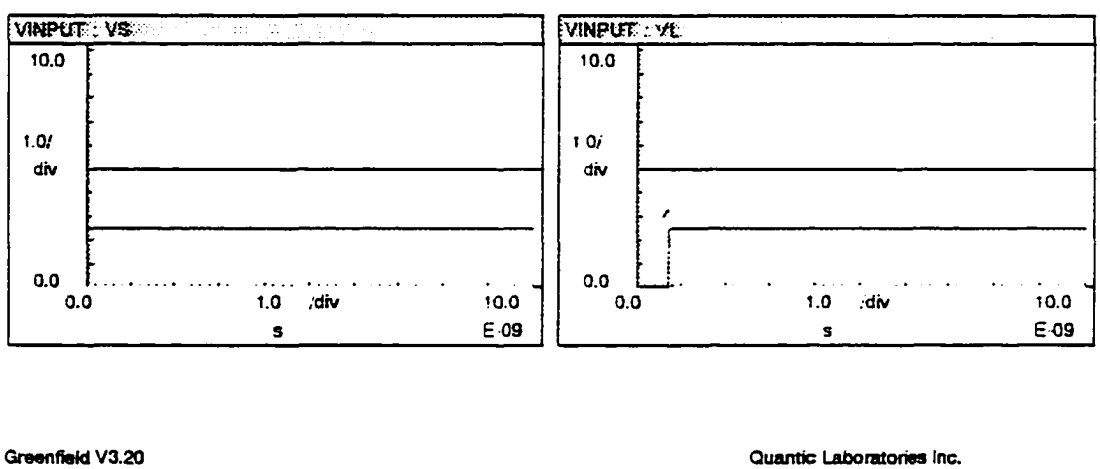

Figure 5.15. Transient voltage response of a matched line

5.6. Modeling

5.6.1. Criteria

At low frequencies the electrical characteristics of a transmission line are insignificant. The line may be accurately modeled as a zero impedance path. At high frequencies, a transmission line has electrical characteristics that depend heavily on the geometry of the configuration. This section defines the terms 'low' and 'high' via a simple criteria based on the physical length of the line and the rise time of the digital signal. The goal is to identify the traces in a digital board that, without proper design, would tend to exhibit problems.

The criteria may be stated in two forms: one comparing the length of the transmission line to the pulse length of the digital signal, the other comparing the time delay of the line to the rise time of the signal. Stated precisely,

The electrical characteristics of a transmission line are significant if the length of the line is greater than one-eighth of the wavelength of the digital signal, or[43]

$$l = \frac{\lambda}{8} \qquad 5\text{-}38.$$

Equivalently, it is stated as

The electrical characteristics of a transmission line are significant if the time delay of the line is greater than the rise time of the digital signal, multiplied by the quantity π/8, or

$$t_d = \frac{\pi}{8} t_r \qquad 5\text{-}39.$$

In other words, if the criteria is true, then the transmission line may tend to pose problems for the digital circuit, and transmission line theory should be used in the analysis and design of the line.

For periodic digital signals such as clocks, yet another rule can be stated. If the propagation delay is greater than one-eighth of the clock period, then transmission line effect must be considered. Recalling that the propagation delay is approximately equal to the line length times the square root of the dielectric constant divided by the speed of light, the rule of thumb is that transmission line design of a signal with frequency f should be considered when

$$l = \frac{1}{8} \frac{c}{f\sqrt{\varepsilon}} \qquad 5\text{-}40.$$

For common values of dielectric constants, a curve shown in Figure 5.16 illustrates this condition.

The inequalities are 'soft' in that, under some conditions, lines much shorter than the criteria may be problematic, or lines much longer than the criteria may operate wonderfully. The problems associated with poorly designed transmission lines are combinations of many factors. The point is that the longer the trace and the higher the frequency, the higher the probability of problems.

The exact definition of the wavelength of a digital signal is unclear, but an approximate number may be obtained from the signal's frequency spectrum. A typical digital signal, representing either a periodic clock train or a random data sequence. The quantity t_{pw} is the pulse width; the quantities t_r and t_f are the rise and fall times, respectively, of the signal. For a periodic clock train, the quantity T is its period. Presenting the information in this format provides a useful "first pass" estimate to the designer.

Another representation of the frequency content of a digital signal is the signal's Bode plot. The spectrum has two poles: one at low frequency due to the pulse width and one at a higher frequency due to the rise and fall time (here assumed to be equal). The spectrum

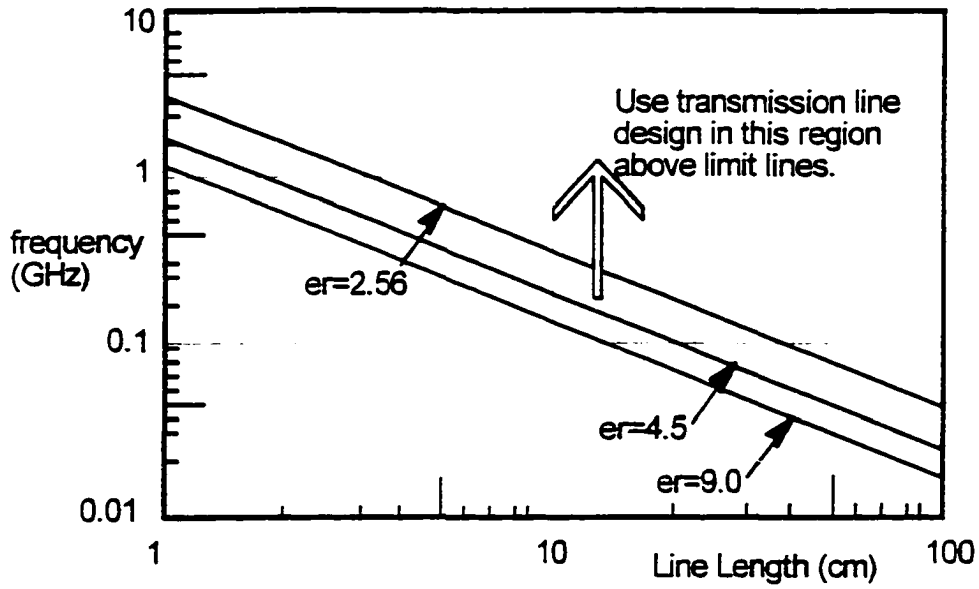

Figure 5.16 Limiting line length for propagation delay

falls off rapidly after the second pole, thus this pole is a reasonable value for the maximum frequency of the signal. The wavelength is then given by

$$\lambda = \frac{v_p}{f} \qquad 5\text{-}41.$$

Note that for today's fastest logic, with rise times around one nanosecond, the lengths necessary to satisfy the criteria are on the order of a few centimeters. Traces having such lengths may certainly exist in circuit boards of reasonable size.

5.6.2. Models

This section is a compilation of several transmission line analysis examples performed using the Greenfield computer aided analysis tool set developed by Quantic Laboratories.

5.6.2.1. Computer Aided Analysis of Circuit Configurations

A two-dimensional analysis of several transmission line configurations can be performed with the tool E.Z.Greenfield2.D. The particular structures that may be analyzed are limited, but it covers all of those commonly found in printed circuits. The configuration is specified through a relatively simple graphical interface. The output is a text file that includes, among other things, three of the four line parameters, the propagation velocity, and the characteristic impedance of the line. Two examples, one stripline and one microstrip, illustrate this analysis procedure. Table 5.3 lists the Greenfield input parameters for each configuration, and Table 5.4 gives representative dimensions for stripline and microstrip constructions.

Figures 5.17 and 5.18 show the resulting cross-sectional diagram generated by the tool, for the stripline and microstrip conductor. The circuitry is modeled as a homogeneous cross-section, with standard values chosen for the relative dielectric constant and the conductivity of the copper traces. Again, this research used boundary element modeling, but other techniques are applicable and offer no degradation of accuracy.

5.6.2.2. Lumped Versus Distributed Transmission Line Models

Greenfield provides the capability for determining electrical effects of the interconnect in high frequency operations. This allows the designers to analyze complicate physical structures to determine the integrity of critical signals in the design. As previous examples clearly demonstrate, the structure and layout of the interconnect clearly affects electrical performance.

Table 5.3. Greenfield transmission line input parameters

XSECTION		
type	stripline	microstrip
DIELECTS		
THICKNESS	21.37 mils	4 mils
MATRL CONST	4.5	4.5
STRIPS		
POSITION	0 mils	0 mils
HEIGHT	10.685 mils	4.685 mils
WIDTH	8 mils	8 mils
THICKNESS	1.37 mils	1.37 mils
Analysis Parameters		
#EZCOND	5.5×10^7 S/m	5.5×10^7 S/m
#EZFREQ	100 MHz	100 MHz

Table 5.4. Dimensions for stripline and microstrip construction

	stripline	microstrip
frequency, f	100 MHz	100 MHz
conductivity, σ	$5.5 \times 10^7\ \Omega^{-1}/m$	$5.5 \times 10^7\ \Omega^{-1}/m$
dielectric constant, ε_r	4.5	4.5
width, W	8 mils	8 mils
height, H	10 mils ($H_1=H_2$)	4 mils
thickness, T	1.37 mils (1 oz)	1.37 mils (1 oz)

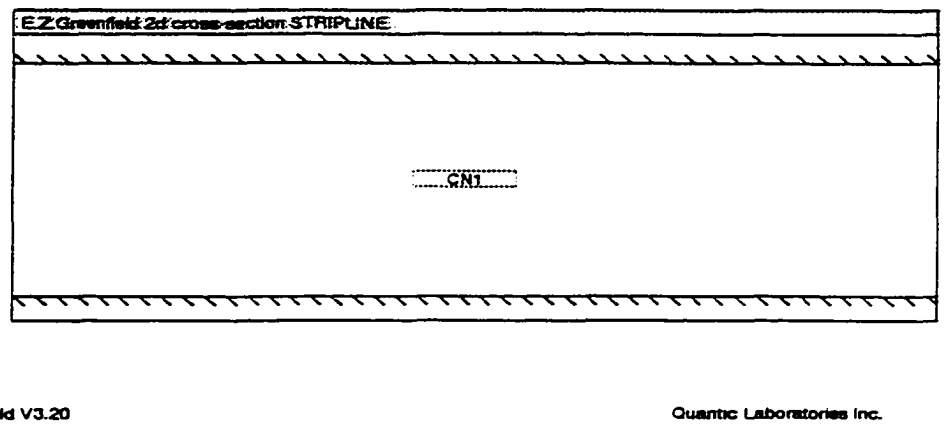

Figure 5.17. Typical stripline geometry in Greenfield

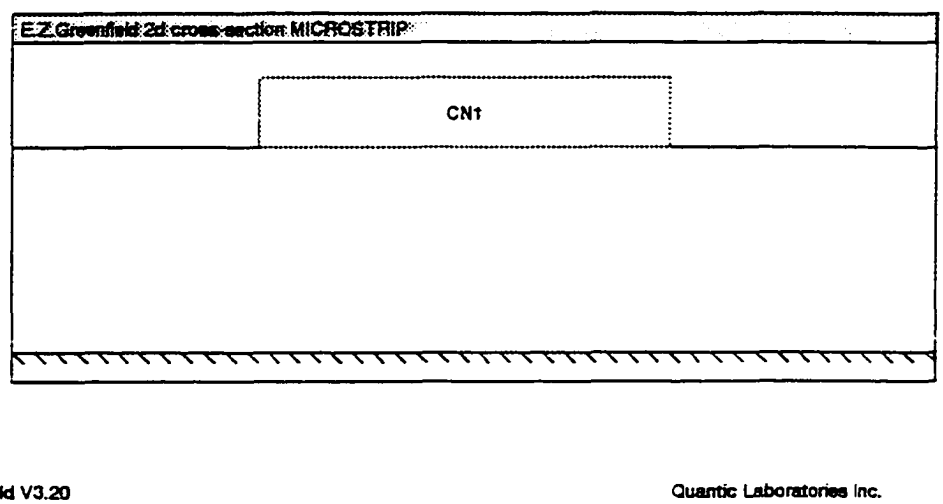

Figure 5.18. Typical microstrip geometry in Greenfield

If the interconnect operates as a short circuit or near short circuit (with small resistance), the signal will propagate from the source to the load with little disturbance. In this case, the time delay of the signal line is insignificant compared to the signal characteristics. For the circuit shown in Figure 5.11, the waveform would be identical for practically any configuration of printed circuit card design, and be a single step function.

The circuit analysis is quite simple, and uses only Ohm's Law, Kirchoff's Laws, and timing analysis.

If the interconnect exhibits the magnetic and electric field properties instead, the analysis is more difficult, and computer aided design must be used. Transmission line analysis, in addition to the basic circuit analysis, must be used to verify operation of the design. Using transmission line analysis, the circuit in Figure 5.11 demonstrates the contributions of the interconnect on the quality of the propagating signal. In practical applications, high speed signals more closely match that of Figure 5.10, rarely looking like perfect step functions that are described by lumped circuit approximations.

5.7. Transmission Line Design

The goal of this section is to summarize the transmission line design procedure for digital circuits. It consists of four steps. The first, discussed previously, is the identification of traces that may require careful design. The second is the selection of a suitable characteristic impedance and a geometry appropriate for that value. The third is the routing of the trace in a manner that preserves the geometry, and thus the characteristic impedance, throughout the entire length of the trace. The final step is the addition of terminations to the trace to minimize the generation of reflection noise.

5.7.1. Characteristic Impedance

A digital waveform has many, often conflicting, requirements. Among these are first incidence switching, monotonicity through the transition region, and minimum reflection noise. The choice of characteristic impedance has some effect on all of these requirements. Therefore, this choice does not represent an optimum value, but merely a compromise.

Typically there exists a range of acceptable values, and the value chosen is the value that best meets the design specifications.

The intent here is not to present a detailed analysis of these requirements and their effects on the choice of characteristic impedance, but rather to give a summary of acceptable impedance values for several digital families. Table 5.5 lists suitable target values within this range for several common families.

Table 5.5. Suitable characteristic impedance values for several digital families

Digital Family	Characteristic Impedance
TTL	50 Ω
CMOS	50 Ω
ECL	75 Ω
BTL	110 Ω

The calculation of characteristic impedance from a given geometry is ideally suited for computer aided design tools. One tool commercially available is Greenfield. In the sections to follow, design information for stripline and microstrip is presented. Closed form expressions are given for each configuration for completeness, but these are rather messy to work with. The best approach of analyzing complex structures is to use Greenfield or some other computer aided design package.

The characteristic impedance of a transmission line is a strong function of both the dielectric constant of the substrate and the geometrical dimensions of the configuration.

These dimensions include the conductor's width, *W*, the distance from the reference plane, *H*, and the conductor's thickness, *T*.

5.7.1.1. Stripline

Figure 5.19 is a dimensional drawing of stripline. The computer aided design tool E.Z.Greenfield.2.D can analyze stripline structures. A complete example of this analysis is included in section. The data presented here is a compilation of analysis runs using this tool, and indicates the dimensional relationships that influence the characteristic impedance.

Table 5.6 lists characteristic impedance calculations for three thickness values: one-half ounce (0.685 mils), one ounce (1.37 mils), and two ounces (2.74 mils). The characteristic impedance *decreases* with increased conductor thickness. The default Greenfield input parameters for Table 5.6 are listed in Table 5.7.

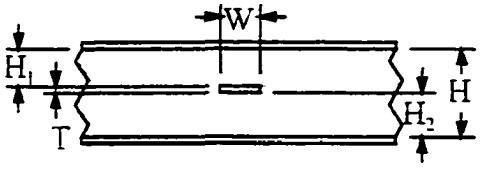

Figure 5.19. Stripline dimensions

Table 5.6. Stripline characteristic impedance versus thickness

Thickness	Characteristic Impedance
1/2 oz = 0.685 mils	49.8646 Ω
1 oz = 1.37 mils	47.6632 Ω
2 oz = 2.74 mils	44.4751 Ω

Table 5.7. Greenfield input parameters for table 5.6

DIELECTS	
THICKNESS (height, H_1=H_2)	21.37 mils
MATRL CONST (dielectric constant, ε_r)	4.5
STRIPS	
POSITION (horizontal position)	0 mils
HEIGHT (vertical position)	10+0.5(T) mils
WIDTH (width, W)	8 mils
THICKNESS (thickness, T)	-
Analysis Parameters	
#EZCOND (conductivity, s)	5.5×10^7 S/m
#EZFREQ (frequency, f)	100 MHz

Closed form expressions for stripline are given below. Most are functional approximations that agree well with measured data. All are strictly valid only when a single dielectric is present. That is, when the dielectric constant of the substrate does not vary within the configuration, and may be considered completely homogeneous with no defects. voids, or gaps The characteristic impedance of symmetric stripline is [41]:

$$Z_o = \begin{cases} \dfrac{60}{\sqrt{\varepsilon_r}} \ln\left(\dfrac{4H}{\pi K_1}\right) & for \dfrac{W}{H} < 0.35 \\ \dfrac{1}{\sqrt{\varepsilon_r}} \dfrac{94.15}{\dfrac{W}{H} + \dfrac{K_2}{\tau}} & for \dfrac{W}{H} > 0.35 \end{cases} \qquad 5\text{-}43$$

$$\frac{T}{1 - \frac{T}{H}}$$

where

$$K_1 = \frac{W}{2}\{1 + \frac{T}{\pi W}[1 + \ln(\frac{4\pi W}{T}) + 0.5\,1\pi(\frac{T}{W})^2]\} \qquad 5\text{-}44.$$

and

$$K_2 = \{\frac{2}{1-\frac{T}{H}}\ln(\frac{1}{1-\frac{T}{H}}+1) - (\frac{1}{1-\frac{T}{H}}-1)\ln[\frac{1}{(1-\frac{T}{H})^2}-1]\} \qquad 5\text{-}45.$$

These expressions are accurate to 1.3 percent under the following conditions:

$$\frac{T}{H} < 0.25 \qquad 5\text{-}46,$$

$$\frac{T}{W} < 0.11 \qquad 5\text{-}47.$$

The characteristic impedance of asymmetric stripline - dual stripline is an example - is

$$Z_o = \frac{2Z_o(2H_1 + T)Z_o(2H_2 + T)}{Z_o(2H_1 + T) + Z_o(2H_2 + T)} \qquad 5\text{-}48.$$

5.7.1.2. Microstrip

Figure 5.20 is a dimensional drawing of microstrip. The computer aided design tool E.Z.Greenfield.2.D can analyze microstrip structures. The data presented here is a compilation of analysis runs using this tool. and indicates the dimensional relationships that influence the characteristic impedance. The default Greenfield input parameters for Figure 5.20 are listed in Table 5.8, with the values given for the geometrical dimensions (trace sizes) as well as for the electrical parameters (material properties).

Figure 5.20. Microstrip dimensions

Table 5.8. Greenfield input parameters

DIELECTS	
THICKNESS (height, H)	4 mils
MATRL CONST (dielectric constant, ε_r)	4.5
STRIPS	
POSITION (horizontal position)	0 mils
HEIGHT (height, H)	4+0.5(T) mils
WIDTH (width, W)	8 mils
THICKNESS (T)	1.37 mils (1 oz)
Analysis Parameters	
#EZCOND (conductivity, σ)	5.5×10^{7} S/m
#EZFREQ (frequency, f)	100 MHz

Table 5.9 lists characteristic impedance calculations for three thickness values: one-half ounce (0.685 mils), one ounce (1.37 mils), and two ounces (2.74 mils). The characteristic impedance *decreases* with increased conductor thickness. This is an important aspect, and one to be considered especially for high speed conductors carrying large amounts of in-rush currents.

The closed form expressions for microstrip are significantly more complex, since it is not a TEM mode structure. Its nonhomogeneous cross-section necessitates the use of an effective relative permittivity, ε_{eff}, and effective width, W_e, in the calculations. The *effective relative permittivity* is an average of the relative permittivities of the substrate and air. For a

Table 5.9. Stripline characteristic impedance versus thickness

Thickness	Characteristic Impedance
1/2 oz = 0.685 mils	47.9591 Ω
1 oz = 1.37 mils	46.3658 Ω
2 oz = 2.74 mils	44.3227 Ω

zero thickness conductor, it is equal to [41]:

$$\varepsilon_{eff,T=0} = \begin{cases} \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}[(1+\frac{12H}{W})^{-0.5} + 0.04(1-\frac{W}{H})^2] & for \frac{W}{H} < 1 \\ \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}(1+\frac{12H}{W})^{-0.5} & for \frac{W}{H} > 1 \end{cases} \quad 5\text{-}49$$

For finite conductor thickness, it is

$$\varepsilon_{eff} = \varepsilon_{eff,T=0} - \frac{(\varepsilon_r - 1)(\frac{T}{H})}{4.6\sqrt{\frac{W}{H}}} \quad 5\text{-}50.$$

The effective conductor width is given by

$$W_{eff} = \begin{cases} W + \frac{1.25T}{\pi}[1 + \ln(\frac{4\pi W}{T})] & for \frac{W}{H} < \frac{1}{2\pi} \\ W + \frac{1.25T}{\pi}[1 + \ln(\frac{2H}{T})] & for \frac{W}{H} > \frac{1}{2\pi} \end{cases} \quad 5\text{-}51.$$

Finally, the expressions for characteristic impedance are

$$Z_o = \begin{cases} \frac{60}{\sqrt{\varepsilon_{eff}}}\ln(\frac{W_{eff}}{4H}) & for \frac{W}{H} < 1 \\ \frac{120\pi}{\sqrt{\varepsilon_{eff}}}[\frac{W_{eff}}{H} + 1.393 + 0.667\ln(\frac{W_{eff}}{H} + 1.444)]^{-1} & for \frac{W}{H} > 1 \end{cases} \quad 5\text{-}52.$$

They are accurate to two percent under the following conditions:

$$0 < \frac{T}{H} < 0.2 \quad 5\text{-}53,$$

$$0.1 < \frac{W}{H} < 20 \quad 5\text{-}54,$$

$$0 < \varepsilon_r < 16 \qquad 5\text{-}55.$$

5.7.1.3. Routing

The discussion up to this point has concentrated on simple point to point connections; one source drives one load. The characteristic impedance of these traces is easily maintained; simply decide on a suitable geometry and provide that geometry throughout the length of the trace. In many applications, however, it is necessary to drive many loads by the same source. One very common example is the distribution of clock signals to multiple points throughout the circuit board. It is very tempting in these instances to *branch* traces to most efficiently utilize board area. One is shown schematically in Figure 5.21.

Unfortunately, in most instances, these junctions are significant impedance mismatches. In other words, a significant amount of reflection noise is generated from them. For example, the effective impedance of two similar transmission lines in parallel is one-half the characteristic impedance of the lines, resulting in reflection and transmission coefficients of

$$\Gamma = \frac{0.5Z_o - Z_o}{0.5Z_o + Z_o} = -\frac{1}{3} \qquad 5\text{-}56$$

and

$$T = \frac{2(0.5Z_o)}{0.5Z_o + Z_o} = \frac{2}{3}\ , \qquad 5\text{-}57.$$

The amplitude of the transmitted voltage waveform is reduced by two-thirds, and the reflected voltage wave actually subtracts from the incident wave. Clearly this could cause problems in the circuit.

One solution to this problem is to make the characteristic impedance of the two branches twice the characteristic impedance of the driving line. The reflection coefficient is zero and the transmission coefficient is one for such a configuration. Unfortunately, this is seldom practical in printed circuits. One reason is that it is difficult to produce traces with widely varying impedances on a single board layer. Another is that, given a constant substrate height, the characteristic impedance is inversely proportional to the width of the trace. Most fine pitch designs tend to push the acceptable technology limits, so the high impedance lines might very well violate minimum width design rules.

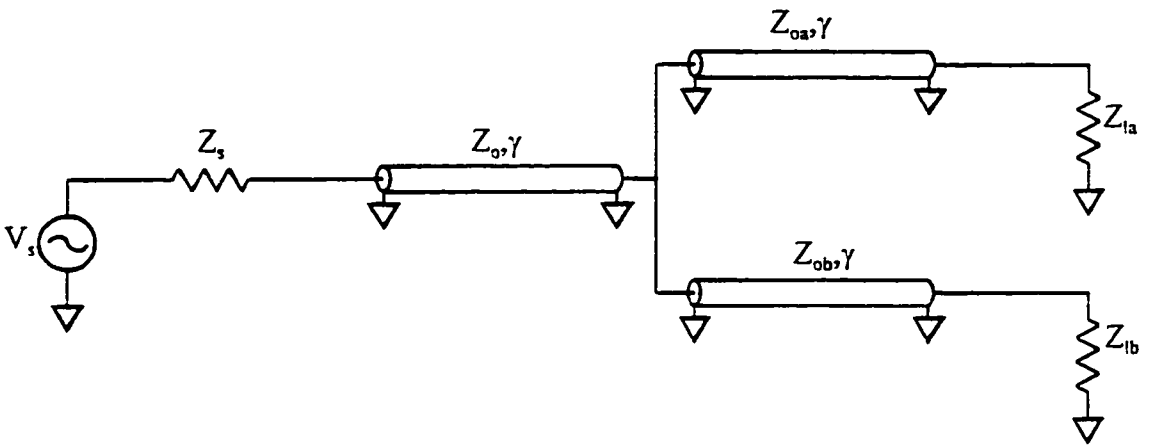

Figure 5.21. Branch in a trace

For multiple loads driven from a single source, branches should not be used in high speed designs. The correct approach to signal distribution is the daisy chain. A *daisy chain* consists of a single transmission line with multiple loads along its length. Figure 5.22 is a schematic representing the multiple loads connected as such.

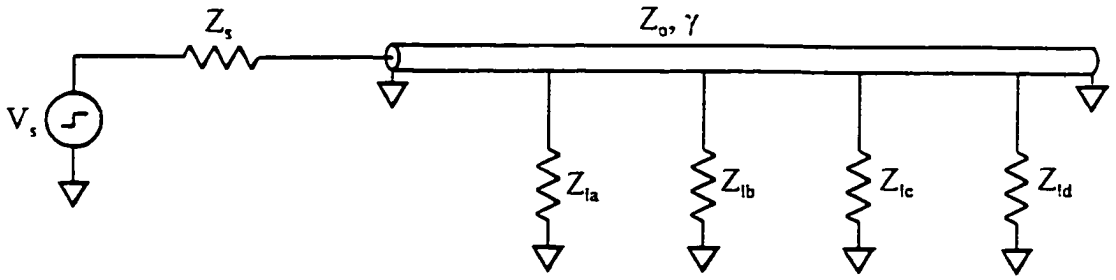

Figure 5.22. Daisy chain

The connections between the main line and the individual loads may include short traces if necessary. Each load and associated short transmission line does present some small impedance mismatch, but in most cases the load impedance is much greater than the characteristic impedance. Thus the reflections caused by the distributed loads are not as severe as those caused by branches.

As a final note, periodically loaded transmission lines have several unique and useful properties. They are not discussed here, but they may provide some interesting options for signal distribution. A thorough investigation on the characteristics of periodically loaded transmission lines requires simulation.

5.7.2. Terminations

The input and output impedances of digital integrated circuits are highly nonlinear and most often not equal to the characteristic impedance of the transmission line connecting them. To minimize the reflection noise caused by these impedance mismatches, some form of transmission line termination is necessary. A *termination* may be located at the source, the load, or both. The purpose of terminations is to correct impedance mismatch, and dampen any reflection from that point.

Several forms of terminations exist, each with its own set of characteristics. Most often, the style is dependent on the routing of the line. For single point to point lines, a *series termination* at the source is often employed. It consists of a resistor in series with the transmission line. Figure 5.23 shows the schematic.

The value of the series resistor should be equal to the difference between the characteristic impedance of the line and the output impedance of the source.

$$R_{series} = Z_o - Z_s \qquad 5\text{-}58.$$

thus presenting to the line an effective source impedance equal to the characteristic impedance of the line. Of course, the value of the output impedance is most often not equal for the high and low states. Thus the value used for the series termination is a compromise, minimizing the ringing caused by a high source impedance as well as ensuring first incidence switching, a problem with a low source impedance. Typical values will range from 20Ω to 40Ω.

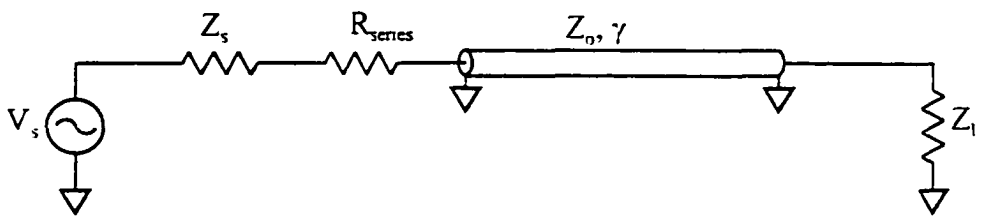

Figure 5.23. Series transmission line termination

With this type of termination, the wave propagates at half amplitude down the line. The impedance mismatch at the load creates a reflected wave that propagates back to the source. The series termination is impedance matched to the line and thus completely damps any further reflections. The input impedance of the load is usually much higher than the

characteristic impedance of the line, giving a positive reflection coefficient. Therefore the reverse wave adds to the forward wave and the line voltage is at nearly full amplitude.

At positions along the line close to the source, the voltage may not reach first incident switching levels until approximately twice the time delay after the gate switches. This may lead to a porch in the voltage waveform, which is an undefined region in most digital logic technologies. For this reason, series terminations are discouraged for transmission lines with multiple loads.

However, the incident voltage is reduced when using the series resistor, since the effective source resistance is raised, and the value of the incident wave is:

$$V_i = V_o \frac{Z_o}{Z_o + R_{series} + Z_s} \qquad 5\text{-}59.$$

Since the radiated energy in EMI is proportional to the square of the voltage, the reduction of the incident waveform is beneficial to EMI concerns, even though it is detrimental to signal integrity concerns. Therefore, series resistors may be used on distributed loads, but the value of these terminators is recommended to be below the value of the characteristic impedance of the line.

Distributed daisy chain line configurations are terminated with an *ac end termination*. It consists of a series resistor and capacitor connected between the end of the line and the reference plane. The function of the resistor is to dampen the incident wave as it propagates through the transmission line structure, while the capacitor acts as a filter element, allowing high frequency components to pass unchanged but low frequency components are blocked and the load may charge to a full value, steady state voltage. Figure 5.24 shows the schematic.

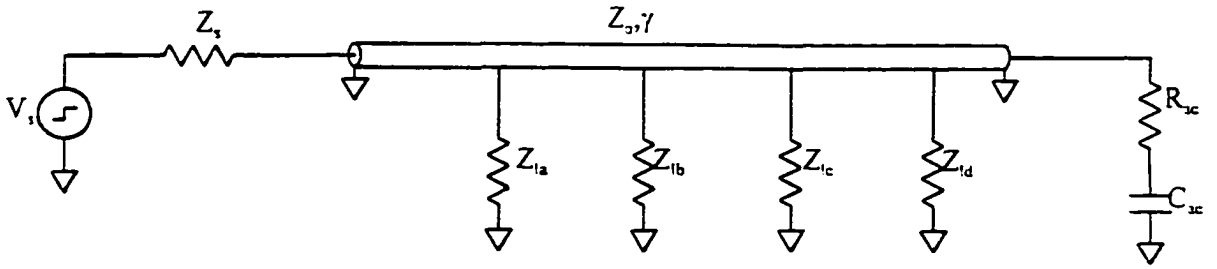

Figure 5.24. AC transmission line end termination

The resistance value is usually slightly larger than the characteristic impedance, and the time constant of the series RC combination is chosen to be much longer than the rise and fall times of the digital signal. For characteristic impedances of 50 ohms, good starting values are close to 68 ohms and 68 picofarads. The location of the termination is not critical, so long as it attaches to the end of the line, after all of the loads.

The operation of the termination is clear when the AC and DC modes are examined. At high frequencies, the capacitor appears to be a short circuit, and the resistive load will dampen the reflected wave since the reflection coefficient will be small. In the DC case (at steady state), the capacitor will be an open circuit, allowing the load to rise to output level of the source.

In this case, the output impedance of the source is usually somewhat smaller than the characteristic impedance of the line, thus most of the source voltage is dropped across the latter. The wave travels down the line at nearly full amplitude. The ac end termination then damps any reflections from the far end of the line. The rise of the signal to its steady state value is then based on the time constant of the RC network.

5.8. Conclusion From Transmission Line Theory

The use of transmission line theory to describe the circuit principles of high speed circuits, or circuits with sufficient electrical length, For the electronics under consideration in this research, the transmission line properties of the external interconnect cabling dictate the magnitude and shape of the waveform propagating from the source of the transient fault.

One method of ruggedizing systems to faults is to adequately shield and filter the external cabling of interconnect systems, to either eliminate the coupling that causes faults to appear on the cabling, or to sufficiently attenuate the energy. To rely on such external provisions is unwise. For this reason, the integrity and reliability of the interconnect must be addressed, and worst case inputs must be assumed.

6. BREAKDOWN OF DIELECTRIC STRUCTURES

6.1. Introduction

To describe the formation of conductive paths through mediums considered to be perfect lossless dielectrics (and as such, perfect insulators), the concepts regarding the breakdown mechanisms in dielectrics are presented. This research, oftentimes concentrating on the formations and reactions of coronas, arcs, or streamers, has been largely been produced on macrostructures (such as power distribution systems, transformers, and insulating devices separating high voltage conductors). The same concepts and mechanisms also apply to the microstructures found in printed circuit card boards.

The observation of the conduction of electricity in dielectrics, such as lightning and the Auroras Borealis and Australis (Northern and Southern Lights) have been noted since the dawn of time. Early experimentation include the Greeks examining the the interaction of bits of straw with a rubbed piece of amber (600 B.C.), and Benjamin Franklin's famous kite experiment of 1752. Formal, controlled experimentation began with the low voltage arc discovered by Humphrey Davy in the early 1800's using a voltaic pile [31]. The continuation of this work led to important discoveries in cathode rays (Plucker), modern atomic theory (Bohr), and to the accidental discovery of x-rays (Roentgen).

The work by Loeb and students of his [29] document the effects and physics of discharge in gaseous, liquid, and solid materials. For the purpose of this research, the effects of gaseous discharge are the most interesting, since the breakdown of the dielectric insulating properties are primarily across the air dielectric, and not through the fiberglass reinforced epoxy resin structure of the circuit card. The purpose of this chapter is to describe the mechanism of the breakdown, and to establish relationship to this research.

6.2. Conduction In Dielectrics

Conducting electricity through a gas is quite different than conducting electricity through a metallic conductor. For metallic structures, the relationship between the applied voltage and the induced current is well described by Ohm's law, with relatively constant resistance. The metal may microscopically be thought of as a lattice arrangement, with electrons free to move about the structure. As the movement occurs, occasional interaction between traveling electrons and stationary ions will translate kinetic motion into heat, as described by resistive loss of the conductor.

However, gases are normally treated as insulators at room temperature and pressure, with a large number of electrically neutral molecules. Each molecule consists of an equal number of positively charged protons and negatively charged electrons, both tightly bound to the nucleus of the molecule. With this arrangement, no free carriers exist to produce a current in response to an applied voltage.

For a gas to conduct current, a large number of electrons or ions must be present. Then, in the presence of an applied voltage, positive ions may travel to the negative electrode and negative electrons may travel to the positive electrode, causing conduction of current. Since the current will have two components, calculating the magnitude is more complicated than calculating the current of a metallic conductor.

Electrons and ions may be emitted from the electrodes or caused from ionization of the molecules in the dielectric. Ionization is caused by the interaction of a moving ion or electron and a molecule, resulting in the liberation of an electron or ion from the molecule. During the flow of current from cathode to anode, both processes occur.

6.3. Breakdown Mechanisms

Electrical discharges in gas are customarily divided into two major types: self-sustained and non-self-sustained. The appreciable difference lies in the magnitude of the applied voltage and the ability for the excited electrons to create secondary processes to replace themselves at the cathode. For further discussion, consider the two terminal system shown in Figure 6.1.

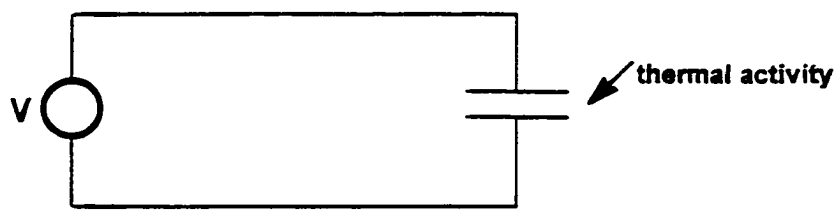

Figure 6.1. Two electrode system

For the system shown, the electric field is assumed uniform. The indication of thermal activity shown in the diagram is to represent the creation of charged elements (electrons and positively charged ions) produced in collisions between gaseous molecules. In all but very small gaps, this is a perfectly valid assumption, since natural ionizing events provide 20 ion-electron pairs/cm^3, which is adequate to initiate mobility from cathode to anode [29]. If no voltage is applied, the rate of formation of ion-electron pairs balances the recombination rate, and the number charged particles is essentially constant. When a voltage is applied, the electrons will drift from cathode to anode, and an electric current can be measured.

The I-V characteristics of the two terminal system is shown in Figure 6.2. At very low voltages (region I of the curve), the current increases with voltage. In this region, the

electrons achieve a drift velocity which is proportional to the voltage. Thus, as the voltage increases, the electrons are collected at a faster rate. Eventually, the electrons are collected as fast as they form, and the current reaches a saturation level (typically in the pA to μA range). Unless additional electrons can be produced, there will be no increase in current.

For a considerable region of voltage, the current is constant. At some point, as the voltage is increased, the current again begins to increase (shown in regions III and IV). These regions are called Townsend discharges, and regions I through IV are collectively referred to as the dark regions or dark discharges, as the density of excited molecules that emit visible light is exceedingly small. To this point, the discharge is considered to be non-self-sustaining.

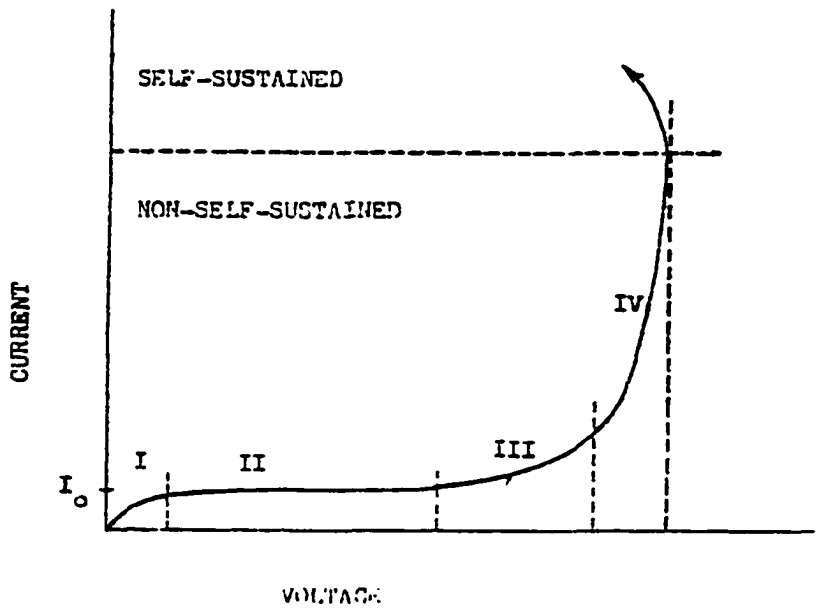

Figure 6.2. I-V Characteristics for two electrode system

Eventually, a voltage (shown as V_S) is reached at which the current begins to increase rapidly. This voltage, V_S, is called the sparking or breakdown voltage. At this point, the current typically has a value of some tens of μAs, and a sudden transition occurs. This transition, oftentimes seen as a spark, may occur with explosive suddenness and marks the change to a self-sustained discharge. The self-sustained discharge is so named since each electron leaving the cathode establishes secondary processes that replace itself with another electron leaving the cathode. The type of discharge and the current are determined by a number of factors, including the gas composition, pressure, circuit impedance, and electrode material. Figure 6.3 illustrates the ionization of the gaseous dielectric by a single electron with sufficient kinetic energy.

For further explanation of the dark regions of operation, and for calculation of the currents using Townsend's ionization coefficients, refer to [29] and [31]. The region of interest for the purpose of this research is the self-sustaining region, and the derivation of V_S.

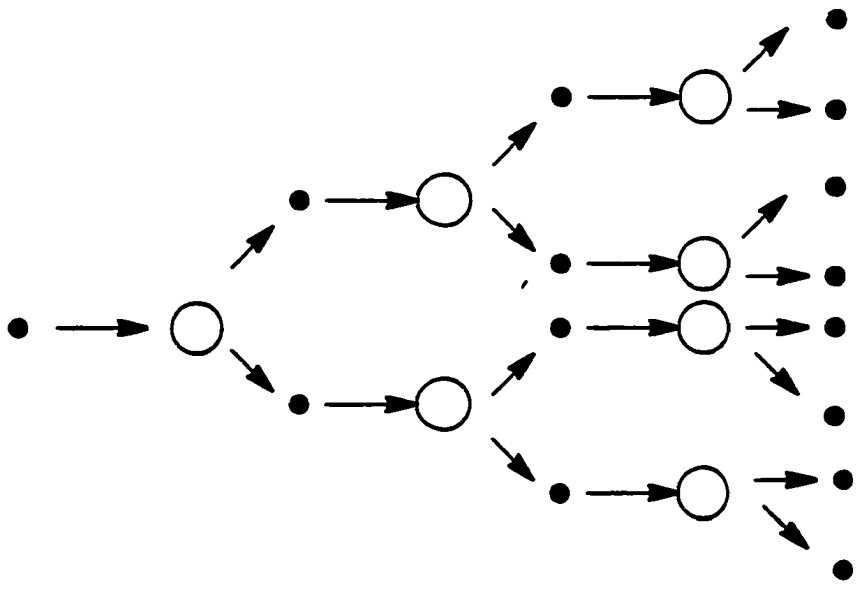

Figure 6.3. Exponential generation of current in gaseous conductor

6.3.1. Breakdown Of Gases

In the analysis of the conduction of a current in a gas, it is noticed that an electron will accelerate due to the applied electric field until it reaches average drift velocity. Traveling at drift velocity, the electron will lose as much energy in collisions as will be gained in acceleration. However, if the electric field is strong enough, the energy spent in collisions will be sufficient to ionize a molecule, freeing a second electron for mobility. The product of this collision will then reach drift velocity until a collision occurs, creating in effect a multiplication of charges. Instead of a single electron reaching the anode (the original electron having left the cathode as a result of ionization at the metal conductor), there will be an exponential buildup of current. This effect is termed *field intensified ionization*

To explain field intensified ionization, an *ionization parameter* α is defined as the number of electrons produced by a single electron in one centimeter of travel in the direction of the applied electric field. This parameter is also referred to as *Townsend's first ionization coefficient* [33]. This parameter specifically addresses the buildup of current in region III of the graph.

The definition of this parameter does not adequately describe the buildup of current in region IV of the curve, or any non-linear regions. To explain these uncertainties, Townsend further proposed the secondary emission of electrons at the cathode due to ion collision. Early experimentation seemed to confirm this, as changing the cathode material or surface conditions altered the current characteristics. *Townsend's second ionization coefficient*, represented by γ, is defined to be the number of secondary electrons emitted per ion collision in the gas volume [34].

For the conduction of current, $e^{\alpha d}$ electrons arriving at the anode as a result of each

electrode leaving the cathode. Therefore, ($e^{\alpha d}$ -1) electron-ion pairs are formed in the gas dielectric space of a uniform electric field as a result of collisions. For the discharge to be self-sustaining, each electron leaving the cathode must be replaced by another as a product of secondary processes. The number of secondary electron is a product of γ and the number of ionizing collisions. Equating the term to unity produces *Townsend's breakdown criteria: [33]:*

$$\gamma(e^{\alpha d} - 1) = 1 \qquad 6\text{-}1$$

Generally, $e^{\alpha d} >> 1$, and the above term can be simplified to:

$$\gamma e^{\alpha d} = 1 \qquad 6\text{-}2$$

If N_0 electrons formed by photoelectric emission leave the cathode as the beginning of the conduction process, each of these electrons will create electron-ion pairs due to collision. The secondary electrons produce further collisions, and the avalanche affect begins. The total number of electrons reaching the anode can be shown to be [35]:

$$N = \sum_{n=0}^{\infty}[N_0\gamma^n(e^{\alpha d} - 1)^n(e^{\alpha d})] \qquad 6\text{-}3$$

If y is defined to be $\gamma(e^{\alpha d} - 1)$, then equation 6-3 simplifies to:

$$N = N_0 e^{\alpha d}\sum_{n=0}^{\infty} y^n = \frac{N_0 e^{\alpha d}}{1-y} \qquad 6\text{-}4$$

Replacing y, and rearranging to solve for current:

$$I = \frac{I_0 e^{\alpha d}}{1-\gamma(e^{\alpha d} - 1)} \qquad 6\text{-}5$$

This relationship describes the current response in separating conductors with a constant electric field. At a maximum distance, breakdown in the dielectric occurs, causing a spark to transfer from cathode to anode. When Townsend's breakdown criteria is reached, the equation is no longer valid, since the equation predicts a steady state condition, and the

breakdown is a transient event. Therefore, the breakdown should be considered a physical realization of the conditions in the conductor gap, and not be treated as a strict mathematical interpretation. Loeb [29] defines classes of operations based on equation 6-2:

a: For $e^{\alpha d} < 1$, the current is not self-sustained, and will stop conduction if the electric field presence is removed.

b: For $e^{\alpha d} = 1$, each avalanche of $e^{\alpha d}$ electrons produces one new secondary electron. This is the sparking threshold for the self-sustained discharge.

c: For $e^{\alpha d} > 1$, more electrons are produced than created at the cathode, and the avalanche is cumulative. Positive ions, due to slower mobility, accumulate near the cathode, producing a secondary mechanism. This condition is shown in the upper region of Figure 6.2, and causes a decay in the voltage, as the surge in current depletes the stored charge, discharging the effective capacitance of the source.

When the effective electric field strength decreases from $e^{\alpha d} > 1$ to $e^{\alpha d} < 1$, deionization occurs. This takes place due to two separate mechanisms: volume recombination and ion diffusion. In the former, free electrons attach to neutral molecules, which then in turn collide with a positive ion, creating two neutral molecules. In the latter, the electrons and positive ions are absorbed into the walls of the boundary where they recombine. While deionization occurs at the same place as ionization during breakdown, the rates may differ substantially. This fact may play an important role in secondary discharges in pulsed power systems or in determining secondary threshold values in repetitive signal systems.

The breakdown of a gas can also be plotted to relate the voltage to the product of the gas pressure and the conductor separation. Commonly referred to as Paschen's law [36], the

relationship states that as the gas density is increased from standard temperature and pressure, the voltage breakdown is increased because molecules are packed closer at higher densities. The electric field necessary to accelerate electrons to sufficient energy to ionizing energy within the mean free path increases. Conversely, the voltage breakdown decreases as gas density is decreased from standard pressure and temperature because the longer mean free path permits the electrons to gain more energy prior to collision. As the density is further decreased, the voltage breakdown threshold decreases until a minimum is reached. Then, as fewer electron-ion pairs are available, the voltage breakdown begins to increase as fewer carriers are available. For air, for bare conductors separated by one centimeter, the DC breakdown voltage at standard pressure and temperature (23° C, 1 atmosphere pressure) is 33kV, while at critical pressure (100 Pascals) the DC breakdown voltage is approximately 326 volts. [36]

6.3.2. Breakdown In Solids

In an ideal solid dielectric, there are no conductive elements, imperfections (voids or cracks), and the material has uniform insulating properties. In practice, solid dielectrics have conductive filaments, voids, thickness variations, and the composition of the material may differ slightly in separate process batches. The selection of the dielectric solid may depend not only on electrical properties, but also mechanical, thermal, chemical, economic, and logistic concerns.

The materials chosen for printed circuit card dielectrics offer higher breakdown thresholds than gaseous dielectrics; however, the solid dielectrics are not self-healing structures. Once a breakdown condition is reached, a catastrophic fault occurs, with the material around the conductive path irreversibly altered. This fact leads to the explanation of

the significantly lower threshold value for surface microstrip circuitry compared to either stripline or embedded microstrip conductors.

Conduction in solid dielectrics is not greatly different from conduction in gaseous dielectrics. The free electrons and positive ions from the lattice structure of the solid must be accelerated in the presence of the electric field. The difference between solid and gaseous structures lies in the deformation of the integrity of the dielectric during conduction. In gaseous structures, the mechanical and chemical structures do not change appreciably during the dark conduction region of the discharge. Probably the most detectable change is a change in temperature due to the thermal agitation of the ions. In solid structures, the mechanical and chemical properties may change drastically, as the mechanical integrity can be greatly compromised if the structure deforms or enters a plastic region. Also, since the solid structure is noticeably more heterogeneous than the gaseous, with voids and regions of dissimilar compositions, thermal gradients can create expansions which lead to mechanical breakdowns such as delaminations or "popcorning".

6.4. Conclusion From Breakdown Theory

For high voltage transients that appear in densely packed printed circuit card assemblies, large electric fields are established around conductive traces. Depending on trace construction (surface microstrip versus embedded circuits), breakdown conditions may be reached due to acceleration of ions and electrons along electric field paths. In this event, the current that is established is self-sustaining until the potential is depleted to sub-discharge levels. In the event of breakdown of gaseous dielectric, the original system is re-established through recombination of ions and electrons, recreating the dielectric. In the event of

breakdown in solid dielectrics, physical deformation of the material may occur, permanently changing the structure.

7. EXPERIMENT AND ANALYSIS

7.1. Objective

The goal of the research is to determine experimentally the effects of high voltage transient inputs on fine pitch laminate structures, determine methods and mechanisms that significantly alter the response to a given input, and improve the understandings of the underlying phenomena to the extent of creating predictive tools for simulation and analysis. To achieve this, a dedicated printed circuit card structure was designed to test waveforms and determine responses. Based on the information presented in earlier chapters regarding crosstalk, transmission line behavior, and dielectric breakdown, guidelines are established and verified for ruggedization of the interconnect to such transients. Finally, a uniform model is to be created that discusses the operation of the fine pitch laminate interconnect during normal operation as well as operation while in the presence of large voltage transients.

As with many other tests involving dielectric breakdown, repeatability of results to exact values and thresholds is difficult. Although absolute repeatability is desired but unobtainable, the values and conditions obtained in the design experiment were consistent within a reasonable range.

7.2. Design Of Experiment

A multilayer circuit card was designed specifically for the series of tests outlined for this research. To determine the effects of the high transient inputs on independent variables, the circuit card allows isolation of inputs to varying trace widths, separations, and distance from reference planes. In addition, both microstrip and stripline structures are investigated. For this experiment, four different circuit geometries were implemented: 4 mil lines with 4 mils of separation, 6 mil lines with 6 mils of separation, 8 mil lines with 8 mils of separation.

and 12 mil lines with 12 mils of separation. For brevity, the geometries will be mentioned as the trace thickness, but the reader needs to remember the importance of the unstated trace separation on the effects discussed.

The waveforms for the testing following the pattern indicated in Figure 7.1 from aeronautical standard DO-160C. These patterns will test not only charged interconnect lines without reflections (as demonstrated by the dampened exponential waveform), but also the worst case charged interconnect with compensations made by distant power source (as demonstrated by the dampened sinusoidal term.) The dampened exponential term is further segmented into short wave and long wave testing, representative of the ability of the external capacitance to hold the charge developed by the external fault.

An external power source capable of delivering large voltage transients is coupled to electrically long external interconnect, injecting transient voltages and currents into the cabling through crosstalk mechanisms outlined in chapter 4. The magnitude and specific waveform characteristics of the injected signals are determined by the transmission line characteristics of the cabling as described in chapter 5. The breakdowns that occur are consistent with the dielectric (both gaseous and solid) breakdown discussion of chapter 6.

Test measurements are taken using oscilloscope probes connected to the printed circuit card under test. Figures 7.2 and 7.3 illustrates the test setup for both direct pin injection testing (non-coupled) and indirect pin injection (coupled) testing. For those waveforms (both dampened exponential and dampened sinusoidal) with magnitudes below sparking threshold, the oscilloscope measurements are representative of the input waveforms, without measurable or noticeable perturbations or attenuations. For those waveforms with

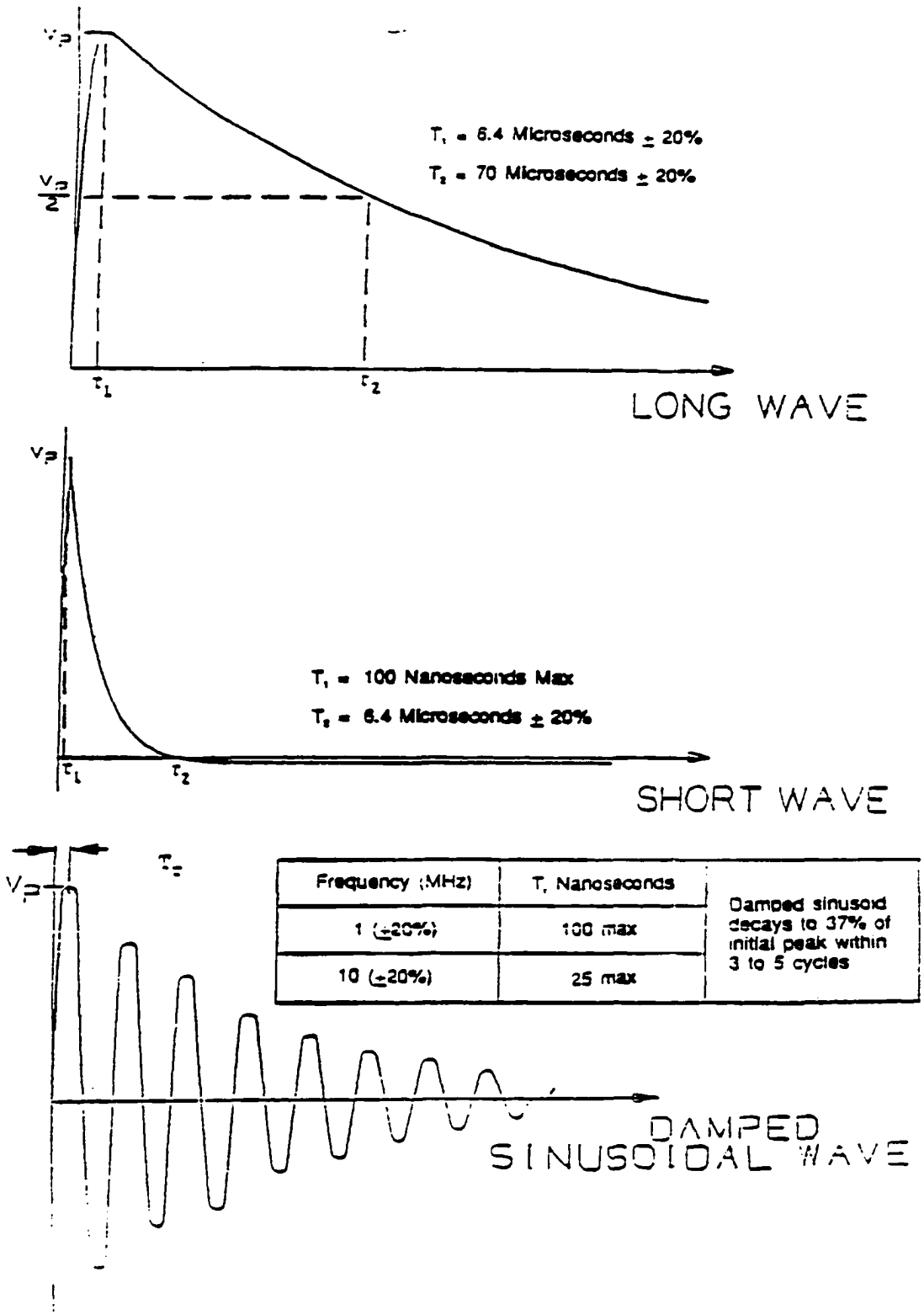

Figure 7.1. Waveforms of DO-160C, section 22 lighting testing

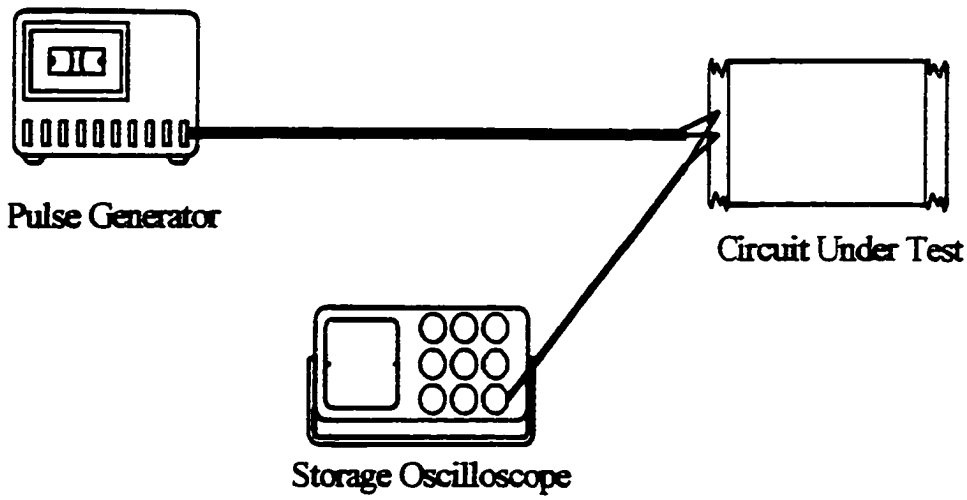

Figure 7.2. Equipment setup for direct pin injection test

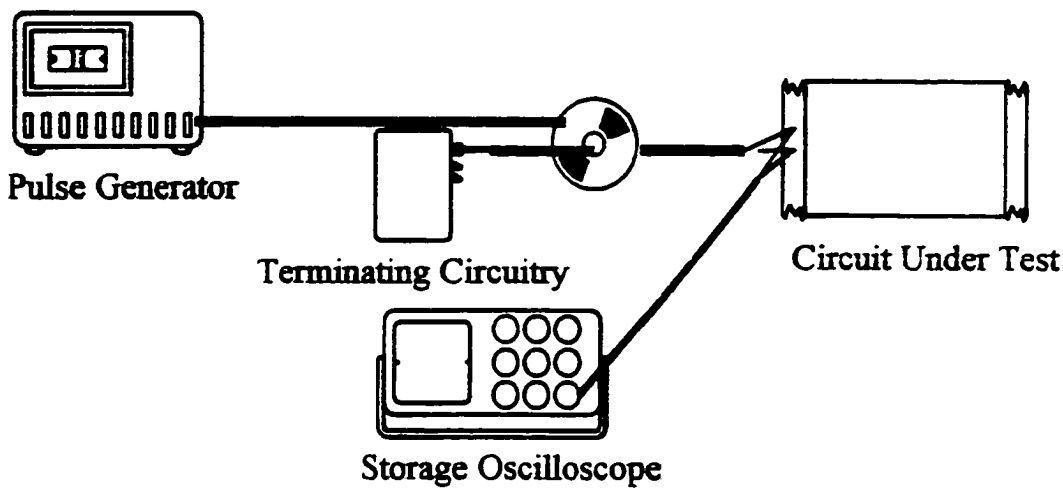

Figure 7.3. Equipment setup for indirect pin injection test

magnitudes exceeding breakdown thresholds, significant perturbations exist, with collapse of voltages and delivered charges.

To determine survivability of the dielectric (the ability to pass transient inputs without collapse of insulating properties), the interconnect structure under test is subjected to

numerous pulses at a given magnitude. The storage oscilloscope measures the waveform as it appears on the laminate structure, and an AM transistor radio is used as a secondary means for detection. Since the frequency of the input waveforms are measurable in the AM radio spectrum, breakdown in the air dielectric is also within the same frequency, and is detectable as static.

7.3. Experimental Results And Comments

From the test data gathered, the survivability of the interconnect appears to be a non-linear function of the fault waveform and of the interconnect design. Tables 7.1 and 7.2 summarize the test conditions and experimental results. Factors that attributed to decreased withstanding voltages during experimentation include: separation of conductors, effective value of dielectric constant, type of input stimulus, and relationship of reference planes to conductors. These factors will be covered in greater detail in the later section describing ruggedization techniques. For the capability of the test equipment and to the limits of the test standard (3200 volts), only the microstrip construction had breakdowns. The embedded microstrip and stripline designs were immune to breakdown to the test limits.

Table 7.1. Measured threshold values for dampened exponential inputs

	Microstrip
4 mil	1300 Volts
6 mil	1395 Volts
8 mil	1440 Volts
12 mil	1600 Volts

Table 7.2. Measured threshold values for dampened sinusoidal inputs

	Microstrip
4 mil	750 Volts
6 mil	1175 Volts
8 mil	1275 Volts
12 mil	1400 Volts

The threshold value for the long wave and short wave exponential input were experimentally found to be similar. Also, the threshold value for the positive going pulse of the dampened exponential was similar in magnitude. An interesting observation is the threshold value of the negative going pulse of the dampened sinusoidal input, which was found to be less than the other magnitudes. This phenomena is due to a polarization effect of the interconnect by the input waveform as it transitions from a positive pulse to a negative pulse in the gaseous dielectric.

Reviewing the transfer of electric current in a gaseous dielectric, both negatively charged electrons and positively charged ions contribute to the charge magnitude. The mobility of the positively charged ions is much less than that of the negatively charged electrons, due to the difference in mass between the two. As a sinusoidal pulse propagates through the interconnect structure, the initial positive pulse attracts electrons to the active conductor, while positively charged ions are attracted to the quiet conductor. As the sinusoidal pulse transitions to a negatively charged pulse, the sign of the electric field is reversed, and the charged ions reverse direction.

Since the positively charged ions have less mobility than the free electrons, the positive ions are less able to move in space between the conductors. As such, a rectification occurs between the two conductors, with positively charged ions concentrating nearer one conductor. This rectification effectively reduces the critical distance between the two conductors, allowing for a smaller electric field (and a smaller imposed launched voltage transient) to initiate a breakdown condition between the electrical conductors.

The defined dampened sinusoidal signal defines an attenuation factor that reduces the transient magnitude to 37% of incident in three to five cycles. When this type of signal is used as stimuli, a single breakdown occurs in the microstrip structure at some point close to the input connector. Experimentally, the dampening factor was reduced to maintain near 100% magnitude for multiple cycles to determine susceptibility due to the rectification. Instead of a single breakdown, multiple breakdowns occurred, as expected. The interesting result of the reduced dampening factor was the location of the breakdown.

Similar to the single breakdown case, the initial breakdown occurred near the input connector, as this is where the microstrip conductors initially start their parallel path. Due to the rectification effects that occur as the input sinusoidal pulse changes polarity, the effective separation between conductors is reduced beyond the point of breakdown. At the point of breakdown, the current flow has eliminated the rectification effect, leaving the separation with a more random distribution of positively and negatively charged elements. The next threshold value is lessened from the previous, and creates a breakdown at a point beyond the initial breakdown point.

This effect of rectification and breakdown at lessened magnitudes causes the effect of the arcing "traveling" up the conductor as it repeatedly collapses the insulation of the dielectric. Figure 7.4 illustrates the effect of the frequency on the breakdown threshold of a system when the fault transient is not attenuated.[36]

The testing and model generation were for particular frequencies as defined in the test standard. As the frequencies of operation change, the breakdown values will need to also adjust, since the dielectric has reduced capabilities of insulation as frequencies increase due to the rectification effects of the gaseous dielectric. This effect is also responsible for the reduced breakdown seen with dampened sinusoidal inputs compared to the breakdown thresholds for the dampened exponential inputs.

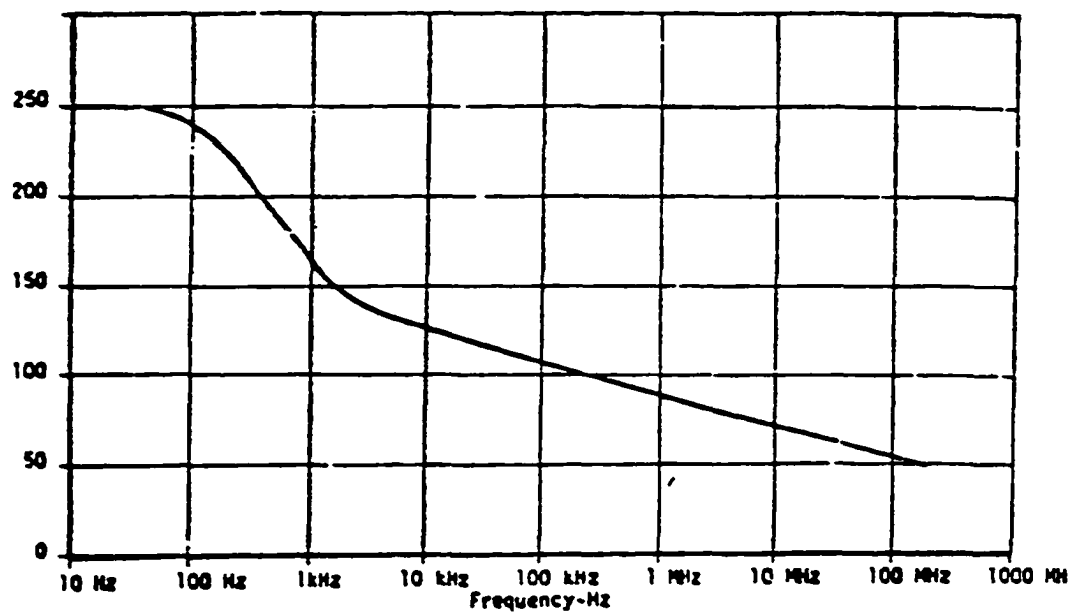

Figure 7.4. Effect of frequency on breakdown threshold voltage

There was some variation between results of the dampened sinusoidal tests when the pulse was driven initially positive as compared to when the pulse was initially driven negative. There are two explanations for this. First, repeatability of the test equipment for negative pulses and positive pulses was difficult to achieve, resulting in a difference in rise times for the two signals. Since the rise time is shown to have an important role in the breakdown thresholds, the test equipment's ability to drive repeatable patterns is shown in the variation. Also, since the cathode and anode are now interchanged, any variation in their construction will become evident, specifically in the shape (sharpness of bend) and surface conditions. This is due to the number of electrons initially emitted from the cathode into the dielectric free space to start the dielectric conduction. Different physical representations of the conductors slightly alters the electric field intensification factor and the number of emitted electrons.

While the edge characteristics of the physical construction of the anode and cathode conductors will vary the value of the breakdown voltage, this variation is negligible with respect to the size characteristics. The governing industry specification for the printed circuit card construction dictates an allowable minimum for the conductor width to be 80% of specified, with further possible degradation in certain areas, such as chip-outs [47]. This variation is greater than the variation due to the conductor edge conditions (for the eight mil case, the sinusoidal excitation altered the breakdown voltage by 25 volts.)

As expected, the separation between conductors was an important factor in the threshold value. The contribution of a solid dielectric, as seen in embedded microstrip circuitry, as an insulating factor was an important conclusion, significantly altering the threshold value of the dielectric breakdown. Its effect on the breakdown had less to do with

the alteration in the electric field strengths as it did in the ability for free electrons to travel along field lines to establish a current path. Since the energy required to force electrons to reach drift velocity values is much greater in solid dielectrics than gaseous, this is reflected in the threshold magnitudes.

7.4. Ruggedization Techniques

For those threshold values that are less than desired for a given set of environmental and system requirements, some means of ruggedization is necessary to increase the breakdown values. A variety of different techniques and approaches may be used, each with relative advantages and disadvantages. Specific implementation choices are left to the system designers.

The problem of the transient breakdown can be analyzed similarly to any other noise problem in electronic systems, with three major components (source, victim, coupling). For the problem to exist, all three must be present. To eliminate the problem, any number of the three may be affected to eliminate the problem. The typical approach is to reduce or eliminate the noise from the source, shield or decrease the sensitivity of the victim, and reduce or eliminate the coupling between the victim and source.

A necessary design element for circuitry operating in high energy transient environments in surge protection circuitry, normally populated as transorbs or crowbar-type elements. The purpose of these shunt elements is to divert the energy to other paths (typically back to the ground or chassis system) and prevent the voltage surges from entering the packages of the integrated circuits. This is an effective approach as long as the suppression circuitry can be placed in series before any potential breakdown feature of the interconnect structure.

For current suppression, ferrous elements are often placed in the interconnect structure, turning current surges into thermal energy. This energy is then passively or actively dissipated, and the components are protected from surges that would otherwise cause internal latch-up or potentially destroy bond wires.

However, in extremely dense interconnect structures, the coupling mechanisms must be examined. Physical limitations of the component placement may create adjacent structures of filtered and unfiltered interconnect. If this occurs, the unfiltered interconnect elements may contain transient energy of sufficient magnitude to breakdown the dielectric separation, bypassing the suppression circuitry and destroying the components of the printed circuit card assembly.

As Tables 7.1 and 7.2 indicate, the threshold value is a function of the trace separation. Changing the interconnect topology to larger conductor geometries will increase the energy level needed to create the breakdown. The disadvantage of this approach is the potential for routing problems as the interconnect may require more layers or a larger circuit card.

Another conclusion from Tables 7.1 and 7.2 is to embed the circuitry in the dielectric, eliminating the surface conductors that have reduced immunity. There are two explanations for this conclusion. The obvious conclusion is the increase in the effective dielectric constant (or permittivity) between the two elements, reducing the magnitude of the electric field. This approach is relatively simple to practically implement, and is a preferred method for ruggedization.

The second component of this technique is the availability from free and mobile electrons needed to initiate the avalanche current. Since the positive and negative ions are

more rigidly restricted in the solid dielectric as opposed to the gaseous dielectric, the energy needed to release secondary electrons from a neutral element after collision with a traveling electron is greatly increased. This effect is not just a property of solid dielectrics, but also of gaseous (non-air) dielectrics with electronegative properties. These gases, such as sulfur hexaflourine (SF_6), are used in sealed structures to provide dielectric insulation without the weight and space penalties of solid dielectric structures. Table 7.3 details the relative effectiveness of air, SF_6, and other gaseous dielectrics for insulation properties.[36]

Table 7.3. Breakdown voltage between bare parallel plate conductors at one atmosphere pressure, one centimeter separation

Gas	Breakdown Voltage (60 Hz AC)	Breakdown Voltage (DC)
Air	23 kV	33 kV
Ammonia	18.5 kV	26 kV
Argon	3.4 kV	4.8 kV
Carbon Dioxide	24 kV	28 kV
Freon 14	22.8 kV	32 kV
Freon 114	64 kV	90 kV
Freon 115	64 kV	90 kV
Helium	1.3 kV	1.63 kV
Hydrogen	12 kV	17 kV
Nitrogen	22.8 kV	32 kV
Sulfur Hexaflourine	67 kV	95 kV

A final ruggedization technique for gaseous dielectrics is to pressurize the system. The increase of pressure reduces the mean free distance between ions, reducing the probability that a free electron traveling along the electric field lines will reach critical kinetic energy levels to release secondary carriers. This effect is noticeable in high altitude aircraft operating in unsealed systems, as the breakdown threshold follows Panshens' law, and a reduced breakdown threshold is noticed [29, 31, 36].

An additional contributing factor that is under investigation in a continuing study is the composition of the solid dielectric material. Solid laminate structures with higher bromine concentrations appear to be more susceptible to breakdown at slightly reduced thresholds. Also, FR-4 materials modified to withstand elevated manufacturing temperatures (with a glass transition temperature of approximately 170°C as opposed to 140°C) appear to be more susceptible to dielectric breakdown. These preliminary results are being investigated in further research outside the scope of this work and appears to be particularly interesting to the power distribution and motor control industrial market.

7.5. Model Construction

The ability to predict the behavior of a circuit or a system prior to construction of prototypes or production units allows the designer opportunities to improve quality, decrease development time, and exhaustively or pseudo-exhaustively test systems in a fashion not practical or possible with physical implementations. For these and many other reasons, the need to create a structured simulation model (of the specific test circuit under test in this study) to predict the behavior of the interconnect during transient operations is important. This model must also work in the event that the transient input is not of sufficient magnitude

to cause breakdown, and the interconnect performs as expected during high speed digital clock rates.

7.5.1. Model Topology

To incorporate the transient model with the normal operation, the model topology is the first question raised. The transient operation, with the collapse of the insulation properties of the dielectric, is oftentimes thought of as a two-dimensional condition, while the transmission line environment is clearly a three-dimensional system, with variations of voltage with respect to both time and space. As stated in the statement of the problem, transmission line systems may be modeled using finite element modeling (FEM), boundary element modeling (BEM), finite difference time domain (FDTD), partial element equivalence circuitry (PEEC), or a variety of other approaches. The approach taken in the model development is that of partial element equivalence circuit (PEEC), which replaces the three dimensional circuit model with a ladder network of discretized resistors, capacitors, inductors, and conductive elements. The PEEC approach directly allows the breakdown elements to be inserted with the standard topology, and also allows for the insertion of other interconnect features and discontinuities. Figure 7.5 illustrates the basic PEEC model element, with the per-unit-length resistance, conductance, inductance, and capacitance. Elements specifically dealing with the breakdown operation will be added to incorporate both modes of operation.

7.5.2. Number Of PEEC Elements

A number of items need to be evaluated to construct the model. One of the first items under consideration is the number of elements needed. This information is constructed from the type of signal under consideration, specifically the bandwidth requirements.

Conventional signal integrity guidelines state the bandwidth of the signal is represented by the following expression [37]:

$$BW = \frac{0.361}{t_r} \qquad 7\text{-}1$$

where BW is the bandwidth, and t_r is the rise time. This expression comes from the spectral content of the digital signal represented in the frequency domain. In the case of the transient waveforms under consideration, the test equipment rise times were no greater than 25ns for the 10MHz waveform 2 inputs. Using this value, the bandwidth of these signals would be 14 MHz.

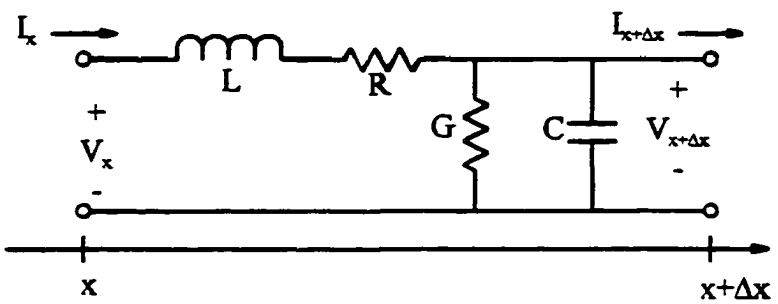

Figure 7.5. Standard partial element equivalence model element

For signals propagating in free space, the frequency and wavelengths are governed by the relationship:

$$\lambda * f = c \qquad 7\text{-}2$$

where λ is the wavelength, f is the frequency, and c is the speed of light (3.0×10^8 m/s). For a signal of 14 MHz, the wavelength would be 21.43 meters. To be considered a transmission line, the distances involved must be less than $\lambda/10$. For the "best" case input, this limit is

2.143 meters. In the test setup defined in this project, the cabling and external interconnect may be tens to hundreds of meters, and such, need to be considered transmission lines.

For the PEEC model to be consistent for normal and transient operations, the rise times of the signals that will enter the interconnect system during normal operation need to be investigated . For heavily loaded digital signals entering the system, rise times on the order of 3.5 ns are acceptable. This correlates to a signal bandwidth near 100 MHz and a wavelength of 3 meters. Lightly loaded signals may have sub-nanosecond rise times. For the unified model, a 1 cm section was chosen, which represents 1% of a 300MHz system. For the test card developed to test threshold conditions for the dielectric breakdown, this would be a ladder of 15 elements. For the external system of interconnect adequately shielded from dielectric breakdown, a transmission line element may be used.

For the transient operation, circuit elements are inserted in parallel to the shunt capacitance and shunt conductance devices. The purpose of these elements is to transition from a high impedance path in normal operation (indicating the conductance of the dielectric) to a low conductance path (indicating breakdown of the dielectric). The primary elements of these additional elements are the threshold voltage of the conductor G_c and capacitor C_c, the threshold voltage for the switch connecting the resistor R_{arc}, and the values for the resistance, conductance, and shunt capacitance, with general topology of a voltage-controlled switching element. These elements, and the topology of the passive element interconnect, is taken from the research in corona. Research in this area [51-55] has been primarily targeted towards distribution systems of high voltage transmission line structures, with the prevalent topology being the cylinder over an infinite plane. Modeling to date has been limited to first order structures (single capacitor and single conductor in parallel), with extensive efforts in place to

avoid corona from causing undue losses to the system. The complete model is shown in Figure 7.6, and has the incorporated elements from the corona theory as well as those elements found in the PEEC model.

Since the embedded microstrip and stripline structures were resistant to breakdown, only unified models for the microstrip case need to be constructed. The unified models for the embedded microstrip and stripline structures for the test conditions of DO-160C are simply the PEEC models for the normal transmission line design. Breakdown conditions depend on breakdown of the solid dielectric, which has greater variability than the gaseous dielectric. This work is an interesting extension, but beyond the scope of this research.

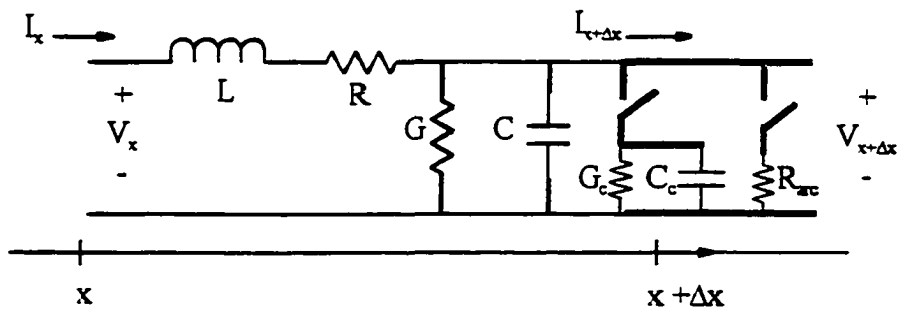

Figure 7.6. Modified partial element equivalence model element

7.5.3. Parametric Values

R, L, C, G: Parameter values for the conductance, resistance, capacitance, and inductance are loaded from boundary element modeling of representative cross-sections. Using the Phyllis program from Quantic labs, the values are calculated using BEM with a base frequency of 100 MHz, a substrate dielectric constant of 4.5 (representative of FR-4 material). While the conductance element of the PEEC ladder element is omitted (indicating

lossless conditions through the interconnect solid dielectric), this parameter has been incorporated into the breakdown element. This value is derived from the material properties specification of the circuit card material [38]. Values for the parasitic values (for a length of one centimeter) are shown in Table 7.4.

G_C: As previously discussed, this element represents the conductance path through the dielectric during the corona phase of the dielectric breakdown. Again, this value is calculated based on research performed on scale model high voltage electrical distribution systems, and represents the loss path for corona. In the concept of the unified model for the microstrip circuit, its importance is to characterize the time constants in place for charging of the corona capacitor. From Peeks law[50], the corona conductance at a given voltage V (where V > the corona onset voltage V_{co}) is:

$$G_c = k_r \frac{(V - V_{co})^2}{V^2} \qquad 7\text{-}3$$

$$k_r = \sigma_r \sqrt{\frac{r}{2h}} (V - V_{co}) 10^{-11} \text{ mho / m} \qquad 7\text{-}4$$

From the equation 7-4, σ_r is the corona loss factor, r is the effective radius of the conductor, and h is the effective distance from the ground.

C_C: This value represents the storage of charge in the dielectric space between the conductive elements. During the breakdown of the dielectric, electrons leaving the cathode strike stationary objects in the separating medium, which in turn release electrons that travel in the direction of the electric field. As this occurs, there exist some electrons and positive ions that exist in the dielectric separation, as well as particles that reach the anode that were from some element other than the interconnect structure. To account for this, a capacitive

Table 7.4. Parasitic values for the PEEC model

	R	L	C	G
4 mil microstrip	48.85 mΩ	1.622 nH	0.6979 pF	57.14 $n\Omega^{-1}$
6 mil microstrip	38.43 mΩ	1.435 nH	0.7785 pF	54.28 $n\Omega^{-1}$
8 mil microstrip	32.36 mΩ	1.294 nH	0.8689 pF	51.57 $n\Omega^{-1}$
12 mil microstrip	34.57 mΩ	1.090 nH	1.0741 pF	48.99 $n\Omega^{-1}$
4 mil embedded microstrip	48.22 mΩ	1.604 nH	1.1481 pF	57.14 $n\Omega^{-1}$
6 mil embedded microstrip	37.93 mΩ	1.420 nH	1.1770 pF	54.28 $n\Omega^{-1}$
8 mil embedded microstrip	31.94 mΩ	1.282 nH	1.2398 pF	51.57 $n\Omega^{-1}$
12 mil embedded microstrip	24.26 mΩ	1.081 nH	1.4074 pF	48.99 $n\Omega^{-1}$
4 mil stripline	46.24 mΩ	1.237 nH	1.4377 pF	57.14 $n\Omega^{-1}$
6 mil stripline	35.82 mΩ	1.063 nH	1.6033 pF	54.28 $n\Omega^{-1}$
8 mil stripline	29.79 mΩ	0.933 nH	1.8011 pF	51.57 $n\Omega^{-1}$
12 mil stripline	22.07 mΩ	0.750 nH	2.2279 pF	48.99 $n\Omega^{-1}$

element is added during breakdown conditions, to represent the storage of electrons that reach the anode from the avalanche excitation.

$$C_c = 2k_c(1 - \frac{V_{co}}{V}) \qquad 7\text{-}5$$

$$k_r = \sigma_c \sqrt{\frac{r}{2h}} 10^{-11} \text{ F/m} \qquad 7\text{-}6$$

From the equation 7-6, σ_c is the corona loss factor, r is the effective radius of the conductor, and h is the effective distance from the ground. Values for the corona elements are included

in Table 7.5. It should be noted again that the values depicted in Table 7.5 are only for those traces built in the microstrip construction. Since the breakdown effect are beyond the level of testing for the embedded microstrip and stripline cases, the corona elements are not applicable and therefore are not calculated or added to the table entries.

Table 7.5. Corona values for the PEEC model

	C_c	G_c	V_{onset} exponential	V_{offset} exponential	V_{onset} sinusoidal	V_{offset} sinusoidal
4 mil microstrip	0.1136 pF	0.2202 pS	1250 V	1100 V	700 V	550 V
6 mil microstrip	0.1606 pF	0.2879 pS	1345 V	1195 V	1125 V	975 V
8 mil microstrip	0.1854 pF	0.3219 pS	1390 V	1240 V	1225 V	1075 V
12 mil microstrip	0.2271 pF	0.3547 pS	1550 V	1400 V	1350 V	1200 V

R_{arc}: Reviewing the construction of the circuitry during arcing, the configuration is that of a cold-cathode arc system, with copper or nickel-clad copper cathode and anode. The current density of a cold-cathode arc circuit is 10^6 to 10^8 A/cm^2 [31], and the element cross-section is the ladder element surface area that would project electrons that would accelerate towards the quiet conductor, approximated by one-half of the surface area of the ladder cross-sectional area. The resistance of the dielectric during the arc would be:

$$R = \frac{V}{J * A} \qquad 7\text{-}7$$

with V being the applied voltage, J representing the current density, and A representing the cross-section of the conductor area.

$V_{on\text{-}c}$: This is the on-value for the voltage-controlled switch connecting the corona capacitance and conductance. Numerically, it was calculated from the research conducted on the corona on-set voltage for conductors separated by an air dielectric. Table 7.5 illustrates the values for the arcing components.

$V_{on\text{-}a}$: The value of this is experimentally determined based on the configuration and geometric representation. The values for the four, six, eight, and twelve mil microstrip circuits are listed in Tables 7.1 and 7.2 for the dampened exponential and dampened sinusoidal inputs. For those geometries not tested in the laboratory (not represented by circuit traces on the test circuit card), this value may be calculated based on maximum electric field strength. Using the Ansoft electromagnetic modeler, the maximum electric field value for the microstrip configuration may be determined using a finite element modeling approach. The values for the arcing components are listed in Table 7.6, and the graph of the maximum electric field strength is illustrated in Figure 7.7. These are for the microstrip construction, as the stripline and embedded stripline cases are not applicable.

Once the maximum electric field magnitude for a given geometry was determined (using a one volt stimulus), the product of the electric field determined through simulation and the breakdown voltage determined experimentally is charted. For the dampened sinusoidal waveform, the product is graphed in Figure 7.8, and the dampened exponential case is graphed in Figure 7.9.

Using a least-squared-error approach, the threshold electric field value is calculated for the air dielectric with each of the input waveforms. For the dampened exponential case, the data points are reasonably linear, which indicates good agreement between calculated and measured values. With the exception of the four mil line data point, the graph for the

dampened sinusoidal waveform also shows reasonable agreement. This outlying value will be discussed in the model verification section.

7.5.4. Model Operation

The simulator chosen for the design is Saber, from Analogy. This analog system provides superior simulation capabilities compared to the available Spice simulation packages available to the researcher, with excellent Monte Carlo analysis capabilities, graphing extensions, plus the ability to alter circuit and model parameters mathematically.

The functionality of the models is separated into the normal and transient modes of operation. In the normal mode, the shunt resistance of the breakdown element represents the conductance of the conductors to ground. The signal is passed unperturbed through the interconnect, and transmisson line effects such as mismatches and reflections are seen. Figure 7.10 illustrates the normal operation.

Table 7.6. Arc values for the PEEC model

	R_{arc}	V_{on_arc} exponential	V_{off_arc} exponential	V_{on_arc} sinusoidal	V_{off_arc} sinusoidal
4 mil microstrip	780 mΩ	1300 V	10 V	750 V	10 V
6 mil microstrip	520 mΩ	1395 V	10 V	1175 V	10 V
8 mil microstrip	367 mΩ	1440 V	10 V	1275 V	10 V
12 mil microstrip	260 mΩ	1600 V	10 V	1400 V	10 V

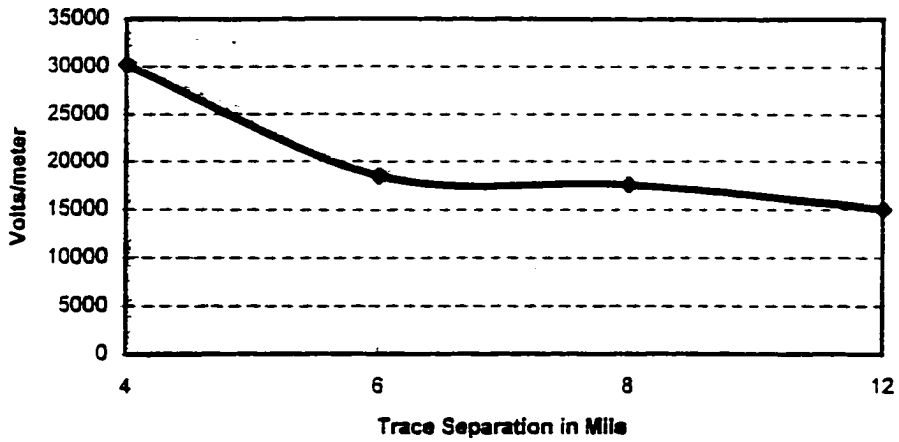

Figure 7.7. Maximum electric field strengths

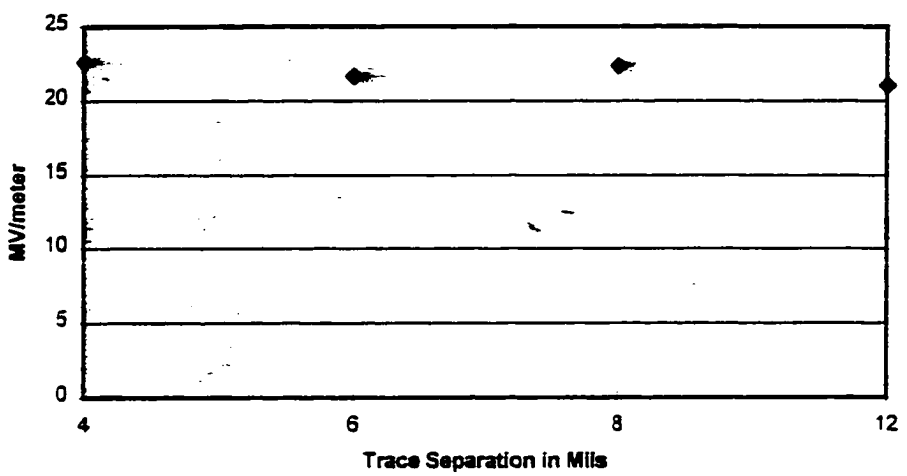

Figure 7.8. Breakdown electric field magnitudes for dampened sinusoidal input

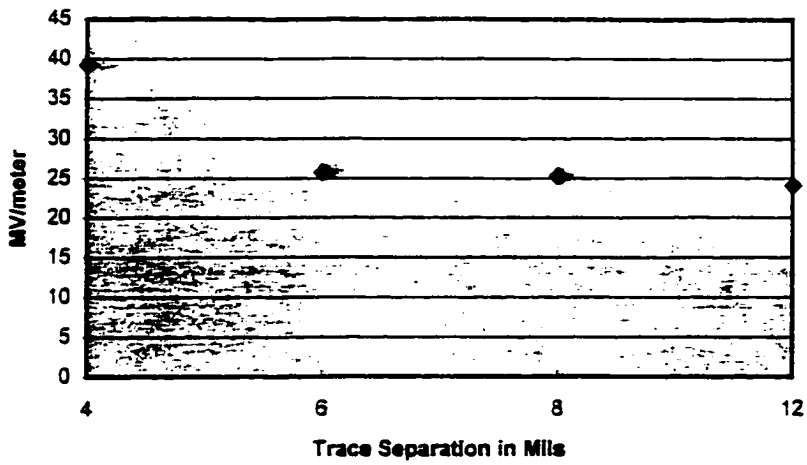

Figure 7.9. Breakdown electric field value for dampened exponential input

The functionality of the models is separated into the normal and transient modes of operation. In the normal mode, the shunt resistance of the breakdown element represents the the interconnect, and transmission line effects such as mismatches and reflections are seen. Figure 7.10 illustrates the normal operation.

In the transient mode, the voltage injected into the interconnect system is greater than the predetermined threshold. The resistance in the breakdown element transitions from a high value to a low value, creating a conducting path from the active conductor to the quiet conductor. This path discharges the energy, introducing a discontinuity to the system, which creates reflections in the transmission line environment. This initial discharge, and the subsequent reflections, propagate through the system until the voltage is reduced to a nominal low value, which then resets the voltage controlled element of the breakdown circuitry. This represents the reconstruction of the gaseous dielectric in physical systems,

with a calculated time lag corresponding to that of the experimental structures [31]. Once this dielectric has been reconstructed, the transmission line environment is re-established, and the model again works in the normal mode.

7.5.5. Model Verification

7.5.5.1. Experimental Verification

The composite models were inserted into the Saber transient analysis package for circuit analysis. The model needs to perform as expected in both the normal modes and breakdown modes. The model is also analytically verified using statistical methods.

The first need to prove that the unified model works as expected in the normal mode; that is, those signals with magnitudes below the threshold conditions pass through the lossless interconnect model without attenuation or perturbations. Figure 7.10 shows the input criteria of the dampened sinusoidal model within the limits of operation of the dielectric's insulating properties, whereas Figure 7.11 simulates the breakdown condition of the dampened sinusoidal input.

Using the calculated value for the threshold condition of the dampened exponential input, the data point of the four mil line was analyzed. The most likely scenario is that the trace used for the circuit cards in the exponential testing was overetched, and the four mil trace is less than specified, and the separation is greater,than anticipated. If this is indeed the case, then the calculated electric field strength was too great, biasing the curve.

For the data point to be approximately linear to the others, the separation should be 5 mils, instead of 4 mils. This was determined by calculating the maximum electric field strength of a 5 mil line using Ansoft, and dividing the threshold electric field strength by the

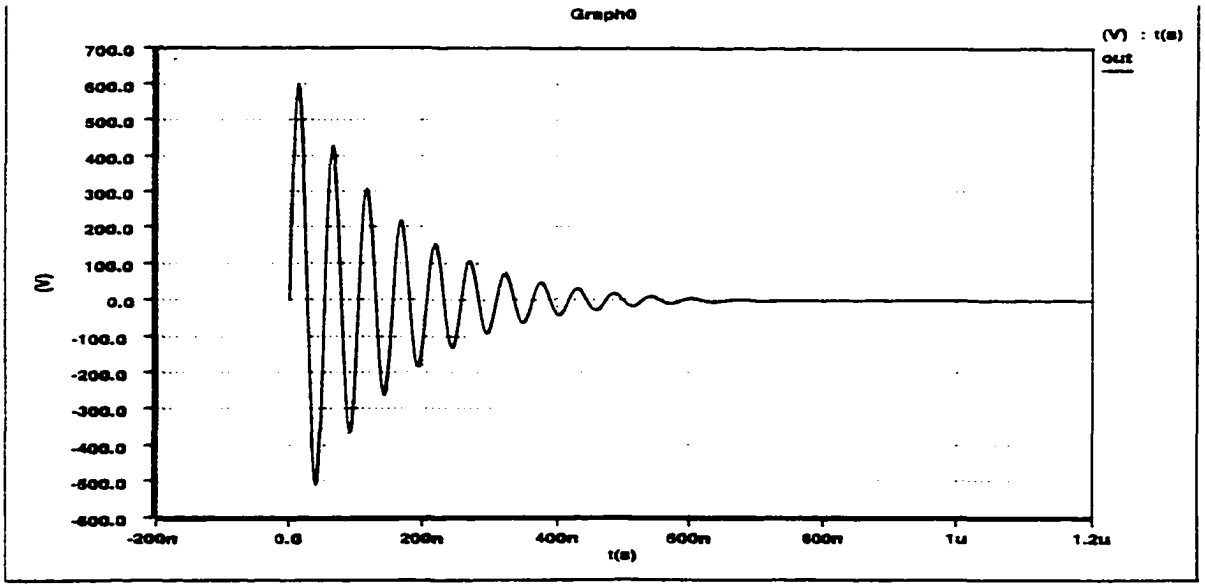

Figure 7.10. Simulation model response of normal operation

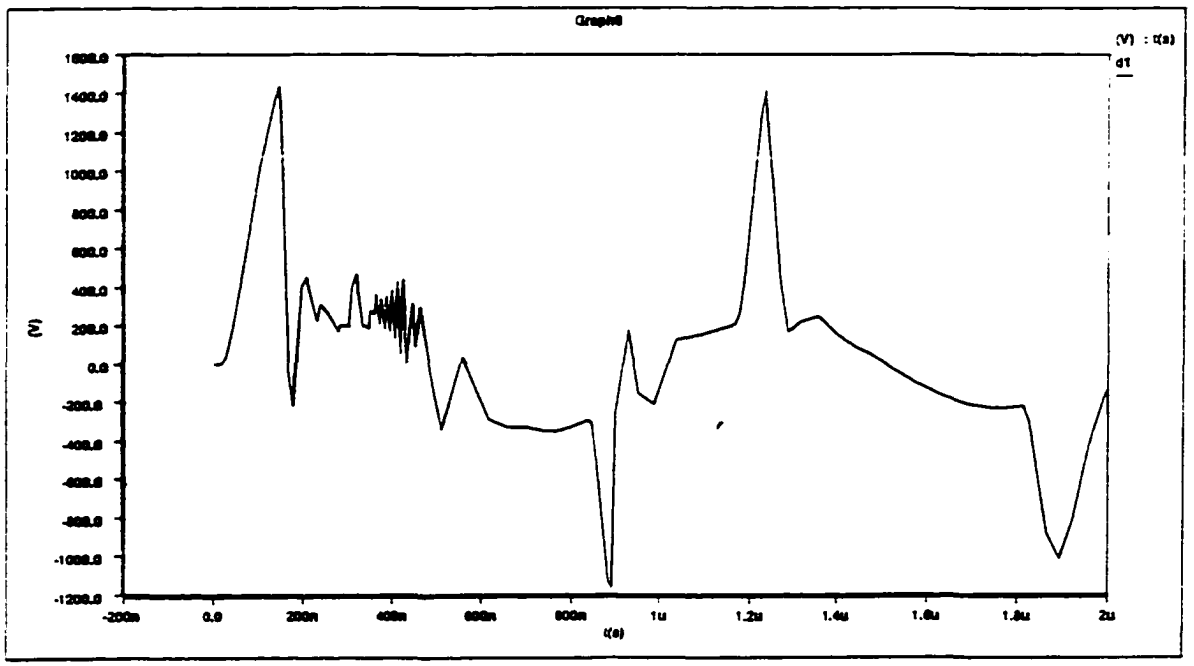

Figure 7.11. Simulation model response of transient operation

experimentally derived value. Microscopic examination of the surface traces show nominal etching of the six, eight, and twelve mil traces, but the four mil trace was at the 80% value, increasing the spacing from 4 mils to 4.8 mils. Adjusting for this, the product of the calculated electric field strength and experimentally derived values is graphed in Figure 7.12.

Verification of the model is shown using statistical methods of linear regression and hypothesis testing. By analyzing the values calculated for the maximum electric field strength for each of the four geometries, a linear function relating the maximum electric field strength to the trace separation is determined. The threshold value of each geometry is compared against the value predicted by the model, with error terms within reasonable allowances for a scientific study. Furthermore, the predicted value of each geometry is then compared against the distribution of data samples taken at each geometry, with hypothesis testing used to verify the validity of the predicted value is not outside of a confidence region of the sample set.

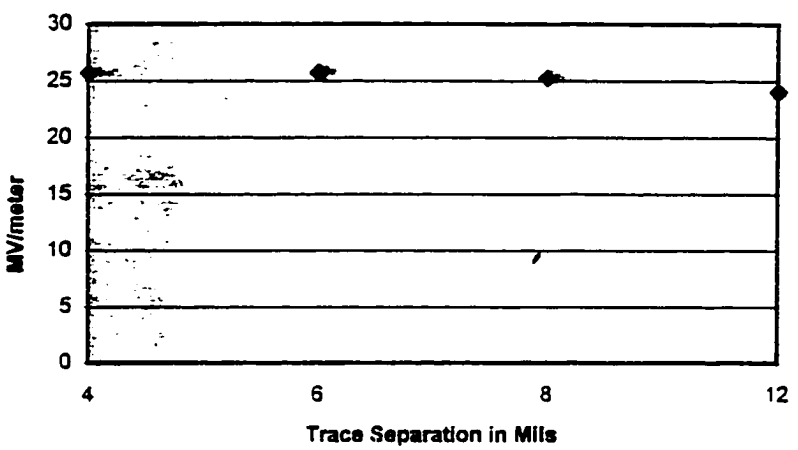

Figure 7.12. Breakdown electric field values for dampened exponential input (adjusted)

7.5.5.2. Linear Regression of the Model

For the breakdown of the air dielectric of microstrip circuitry, the critical term for breakdown is the maximum electric field strength, with one circuit excited and the other passive. To determine the maximum electric field strength, the interconnect profile is analyzed using finite element methods to determine the maximum electric field value for a unit voltage, and then is multiplied by the threshold voltage determined experimentally to determine the maximum electric field present in the circuitry at the time of breakdown. Since the breakdown mechanism is predicted to be only a function of the electric field strength and the air pressure (Paschen's Law), the maximum electric field is expected to be constant, independent of the trace separation.

To best determine the value for the maximum electric field strength, the statistical approach of weighted linear regression is used, where parameters are estimated via least squares [56,57]. By employing this approach, the assumption is made that the maximum electric field strength is a linear function of the separation, and may be graphed as $Y = \beta_o + \beta_1 X$, where Y is the maximum electric field strength (in MV/m) and X is the space separation (in mils, or 0.001 inches). For the exponential and sinusoidal case, β_1 is expected to be zero, and β_o is then considered the critical electric field strength.

For the dampened exponential case, the agreement was poor, with the four mil point dramatically higher than the other data points. Using the critical value of the maximum electric field strength based on the regression of the other three data points, the poor agreement could be explained if the calculated electric field strength from the interconnect profile was less than calculated, equal to that of a interconnect separated by 4.85 mils, not 4.0 mils. The interconnect of the circuitry used in the exponential and sinusoidal tests were then

physically analyzed to determine the actual separations. In the sinusoidal circuit cards, and for the 6 mil, 8 mil, and 12 mil traces of the circuit cards used for the dampened exponential tests, the actual interconnect was at nominal values. However, the interconnect of the four mil trace in the circuit card used in the dampened exponential excitation was overetched, resulting in a separation of 4.8 mils, not 4.0 mils. Recalculating the maximum electric field value for this trace produces a value in close agreement with the calculated values for the other interconnect.

Using the calculated electric field strength of the 6, 8, and 12 mil traces allowed prediction of the breakdown value of the 4 (later determined to be 3.2) mil trace, and proved the predictive ability of the breakdown mechanism of the model. In a similar exercise, the values for the 3.2, 6, and 8 mil lines are used to calculate the expected breakdown of the 12 mil line for the exponential case. Tables 7.7 and 7.8 outline the regression results and error calculations, using the linear regression analysis.

Using the regression analysis, the breakdown threshold voltage experimentally determined can be compared against the value predicted by the least-squared-error term. For the example of the 4 mil line of the sinusoidal input, the data points for the 6, 8, and 12 mil lines were considered to create the equation $Y = \beta_o + \beta_1 X$, with the coefficients shown. By comparing the calculated value from this equation (using the calculated coefficients) to the experimentally derived value, an error term is developed, expressed as a percentage with respect to the predicted value. The agreement seems rather good, since the fitting errors are <= 3.0% for the sinusoidal case and <=1.7% for the exponential case.

The difficulty of a statistical comparison using a small number of data points is the variance is not accurately determined. For a study for manufacturing purposes, large samples

Table 7.7. Regression terms and error terms for the dampened exponential input

	β(1)	β(0)	%e (4 mil)	%e (6 mil)	%e (8 mil)	%e (12 mil)
all points	-0.21986	26.81279	1.644003	-0.84874	-0.7827	0.514826
6,8,12 mil	-0.254	27.18596	1.627551	-0.84317	-0.77959	0.515604
3.2,8,12 mil	-0.23719	26.91985	1.64076	-0.84864	-0.78369	0.516984
3.2,6,12 mil	-0.22344	26.77088	1.64737	-0.85086	-0.78491	0.516639
3.2,6,8 mil	-0.06167	25.88574	1.670937	-0.84801	-0.77227	0.494942

Table 7.8. Regression terms and error terms for the dampened sinusoidal input

	β(1)	β(0)	%e (4 mil)	%e (6 mil)	%e (8 mil)	%e (12 mil)
all points	-0.30869	24.45998	2.605875	2.909787	-1.68046	-1.36974
6,8,12 mil	-0.28252	24.30751	2.611249	2.909203	-1.67612	-1.35917
4,8,12 mil	-0.32369	24.76441	2.578734	20882446	-1.66648	-1.36158
4,6,12 mil	-0.18692	23.24077	2.690695	2.974064	-1.69939	-1.35396
4,6,8 mil	-0.26557	23.99256	2.639393	2.936899	-1.68987	-1.36645

would be needed to determine the value of the variance to an acceptable level. In this study, however, a large number of samples were used to determine the breakdown threshold voltage for the small number of geometries under consideration. The verification of the model is made using N-1 points to determine the value of the N^{th} sample breakdown condition to a value within expectation of a scientific study, with N=4 in this analysis.

7.5.5.3. Hypothesis Testing of the Model

Linear regression is used to determine the validity of the coefficients used to create the linear model relating the trace width and trace separation to the maximum electric field strength at breakdown. These values used in determining the coefficients are based on the experimental data of the breakdown voltage for each geometry multiplied by the maximum electric field value for each geometry determined through simulation based on a unit volt excitation. The purpose of the hypothesis testing is to verify the computed breakdown voltage determined at each geometry using linear regression to the data points determined experimentally for the population of circuit cards under test.

For both experiments (sinusoidal and exponential), eight circuit cards were used, identical components on a single panel, ensuring uniformity between samples to the levels of fabrication accuracy. During the testing, a test voltage is selected, and ten pulses are injected at the selected magnitude, with either the presence or absence of breakdown recorded. The test voltage is increased incrementally until breakdown occurs consistently for each board under test.

For the multitude of the test pulses, the number of additional breakdowns produced for a given voltage is defined to be the breakdown term for each voltage. These values are statistically analyzed, to produce mean and variance calculations for the population of the breakdowns, with the sample size of the test being 80 (eight circuit cards under test multiplied by the test voltage with ten injected pulses creating breakdown.)

In the hypothesis testing, the hypothesis is that the calculated breakdown voltage produced by the coefficient terms from linear regression is the true population mean, and cannot be proven to lie outside the standard distribution of the sample population. To assert

this hypothesis to be false with a confidence of 95% (and to disclaim the value for breakdown produced by the model based on the sample data), the t value from the analysis must be greater than 1.994 or less than -1.994. The values for the hypothesis testing are shown in the Tables 7.9 and 7.10.

Table 7.9. Sample statistics and hypothesis test coefficients for the dampened exponential input

	3.2 mil trace	6 mil trace	8 mil trace	12 mil trace
Threshold Voltage	1300	1395	1440	1600
Mean Threshold Voltage	1307.5	1404.5	1438.875	1603.75
Standard Deviation (volts)	17.854	31.091	20.916	25.951
Predicted Threshold (volts)	1309.554	1397.33	1422.49	1607.442
t = (Mean-Predicted)/StdDev	-0.1151	0.2306	0.7834	-0.1423

7.5.5.4. Conclusions of the Model Verification

Using statistical methods that are well accepted in the engineering and scientific communities, the model produced for the breakdown conditions has been verified for the threshold value of the collapse of the air dielectric. In the two part experiment, each component has been verified, which completes the verification test for this component for the complete model. The first component of the model, the linear expression relating the maximum electric field at the point of breakdown, has been verified using linear regression to prove predictive ability for the geometries under consideration. Finally, the value computed

at each geometry has been verified within the sample data to demonstrate the ability for the computed data to represent the population mean within the confidence interval of at least 95%. As an additional extension, the model was used to correct the information presented, predicting the actual dimension of a circuit element after the test data indicated large discrepancies between expected and analyzed.

Table 7.10. Sample statistics and hypothesis test coefficients for the dampened sinusoidal input

	4 mil trace	6 mil trace	8 mil trace	12 mil trace
Threshold Voltage	750	1175	1275	1400
Mean Threshold Voltage	762.375	1179.25	1281.75	1413
Standard Deviation (volts)	15.2679	39.489	19.829	30.1828
Predicted Threshold (volts)	745.790	1196.084	1254.942	1393.889
t = (Mean-Predicted)/StdDev	-1.0863	-0.4263	1.3520	0.6332

7.5.6. Accommodation For Variation

The use of the Saber tool suite for the modeling of the interconnect structure allows variation of the modeling, better representing the imperfections and abnormalities of physical structures. The key to this is the parameterization of the interconnect values, passing the entries as preset variables instead of constants.

In the first situation, Monte Carlo analysis techniques may be used to statistically alter the threshold values, representing the variation in trace separation or the presence of

discontinuities that could alter the electric field strength in regions of the dielectric. In the second case, the key characteristics can be mathematically related to time to represent the polarization of the interconnect, and allowing the rectification effects to be modeled. In both cases, the strength of the simulation package allows flexibility and broadens the range of applications for the models.

7.6. Conclusion From Analysis

For the stripline and embedded microstrip conductors, no additional design effort is needed to ruggedize the circuitry to withstand the transients that might enter the system due to lightning or other external faults. Per the test methodology of DO-160C (section 22), the interconnect will safely propagate the signals without suffering damage or breakdown.

Microstrip circuitry, however, is not immune from damage or from breakdown. Depending on the waveform (either sinusoidal or exponential decay), the threshold value may be less than the specific test conditions and requirements, placing the electronic system in jeopardy. The interconnect must be analyzed to ensure the levels of operation during a fault transient meets design criteria.

For a given waveform, the threshold electric field can be approximated to a constant value, independent of geometry. To determine the maximum voltage that may be withstood, the electric field value would be computed using field solvers (calculated for a standard one volt input), and the threshold voltage would be calculated by dividing the threshold electric field by the computed electric field value for the one-volt input. This method was verified, by predicting the actual separation of the interconnect designed to be four mils wide in the test cards used in the dampened sinusoidal testing and standard statistical techniques, and through the use of statistical methods employed in similar experiments.

To simulate the effects of a given voltage on the interconnect topology, a description of the model construction is given. Although the specific model used in this analysis is Saber (from Analogy), Spice may be used with little or no modification to the model. Tables in the discussion of this text presents values for the component entries. A full copy of the simulation files may be obtained by contacting the author at joeljorg@prairie.nodak.edu.

8. CONTRIBUTIONS

8.1. Summary of Contributions

The analysis from this research provides:

i) A detailed account of maximum allowable voltage of fault transient of fine pitch interconnect designs on circuit traces represented by parallel and mitered (45^0) circuits.

ii) A detailed methodology to provide increased survivability for these fine pitch interconnect designs in the presence of high energy transients.

iii) The development of empirical models to predict the breakdown of interconnect due to high energy transients in circuit cards. These models are restricted to fine pitch interconnects that have mitered (45^0) entrance circuits from fine pitch and standard pitch connectors and to waveforms as defined in DO-160C (detailed in this document).

8.2. Detail of Expected Contributions

8.2.1. Uniqueness

The study of signal integrity centers on propagation of high-speed signals under normal operating conditions, ensuring proper signal levels and transitions with minimal interferences. The focus of this concentration is the interconnect and passive elements of the design.

The study of EMI/EMC, and related requirements (HIRF, TEMPEST) focuses on the emissions and susceptibility of radio frequency energy at the system level at normal and transient operation. Primary elements under consideration are connectors, cabling, and wire harnesses.

The focus of the proposed research is to fill a void in the two areas of research. This study will examine the effect of transient operation, in the form of high energy input waveforms, on the interconnect structure normally examined during signal integrity analysis, accomplished by the design and analysis of a fine pitch circuit card using parallel and mitered interconnects. The result of this research furthers the knowledge sought in the survivability recommendations of EMI consultants, and provides simulation models for the specific test case for the signal integrity community that combines the normal and transient modes of operation.

8.2.2. Deliverables

The results from this research can be used to ensure that system faults, system failures, and system damage can be mitigated or eliminated completely through proper interconnect design that will allow for fault transients. First, the derivations and constructions of partial element equivalence models will provide a greater understanding of the response of fine pitch interconnect structures and geometries to high transient voltage conditions, not only of the ability to survive, but also mechanisms for ruggedization. In systems such as avionics equipments where reliability estimates for expected time to failure are necessary, this research may provide insight into a fault mechanism not yet detailed. As the frequency of fault conditions increase, some adjustment to the reliability predictions must be made.

In addition, this research developed fault models for the interconnect test vehicle, allowing simulation of the transients for breakdown, as well as a methodology to create other models to accommodate geometries of similar microstrip construction. As the geometries of fine pitch interconnections change with advances in technology, the models can be either

altered or used as a starting point for new models. This will advance the simulation capability of passive circuitry constructed in laminate interconnect, and improve the signal integrity and electromagnetic interference/electromagnetic compatibility predictive analysis. By having a solid understanding of the signal integrity/EMI/EMC issues before prototypes and production units are constructed, the cost of the system is reduced and time to market response is improved.

A majority of the work for this research was completed during my employment at Rockwell Collins, Incorporated as part of a research initiative to verify the safety of fine pitch laminates for embedded applications in avionics environments. To this extent, the interconnect of fine pitch laminate constructions were subjected to the limits of the manufacturing, electrical, and environmental conditions to verify proper operation for flight-critical safety applications. With the emphasis of applied research, the design of the experiment and the methodology of the testing and analysis is geared towards the industry standards applicable to the customer's environment.

The testing of the circuits uses equipment and components not available at Iowa State University, with dedicated high voltage, high speed circuits and test equipment used. The results of the testing for limits of operation and methods for ruggedization are directly used in the establishment of design rules for Rockwell engineers during printed circuit card design, and to Iowa State researchers in the areas of laminate interconnect in environmentally stressful applications.

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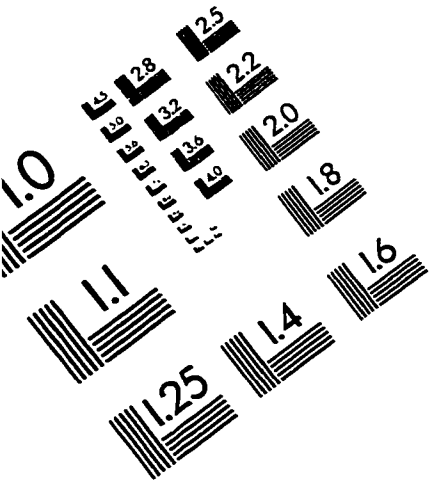
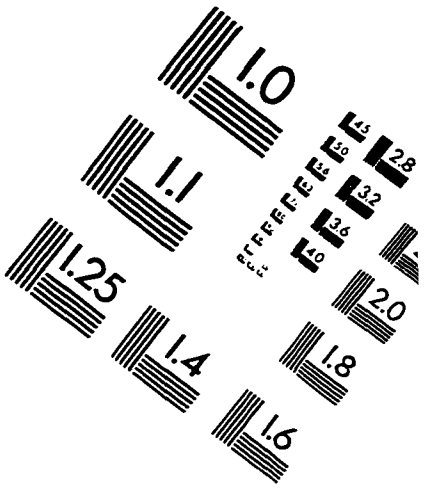
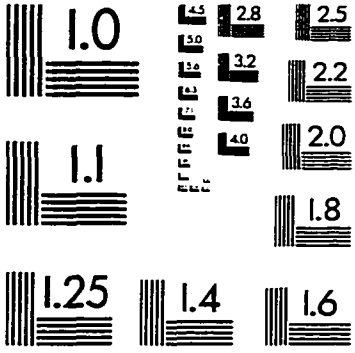
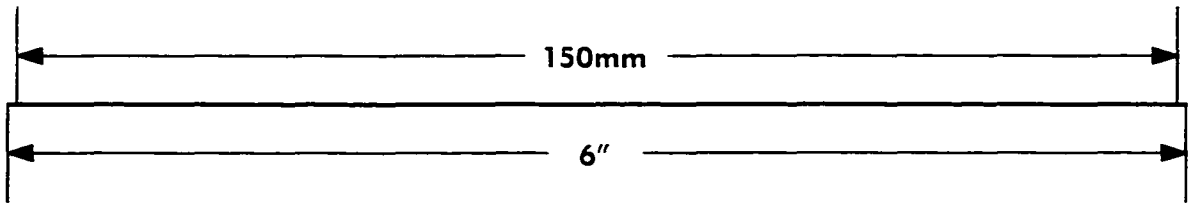
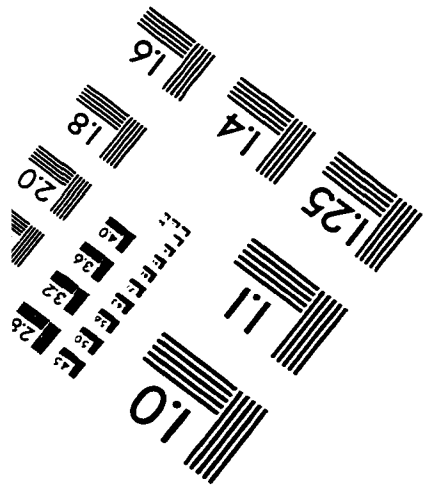
IMAGE EVALUATION TEST TARGET (QA-3)

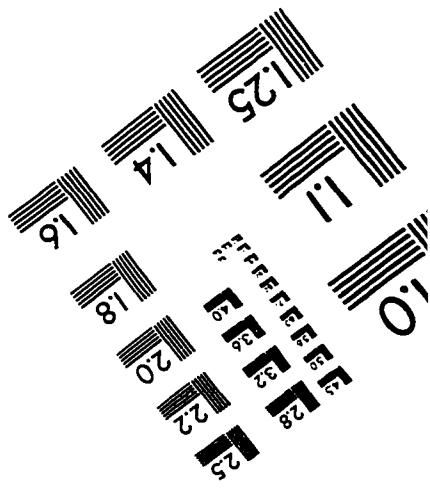












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